# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

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| Attorney Docket No. | 980233B | Total Pages | |
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First Named Inventor or Application Identifier

Nirio FUKUSAWA et al.

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PAGE 1 OF 3

APPLICATION ELEMENTS FOR:
METHOD AND MOLD FOR MANUFACTURING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, AND METHOD FOR MOUNTING THE DEVICE

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1. [X] Fee Transmittal Form (Incorporated within this form)
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2. [X] Specification Total Pages [254]

3. [X] Drawing(s) (35 USC 113) Total Sheets [131]

4. [X] Oath or Declaration Total Pages [8]

a. [ ] Newly executed (original or copy)

b. [ X ] Copy from prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 17 completed).

i. [ ] Deletion of Inventor(s)
Signed statement attached deleting inventor(s) named in prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [X] Incorporation by reference (usable if box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement Verifying identity of above copies

**ACCOMPANYING APPLICATION PARTS**

8. [X] Assignment to FUJITSU LIMITED, Kawasaki, Japan in the prior Application Serial No. 09/029,608, filed on March 15, 1998 has been recorded at Reel 9183, Frame 0260 on May 15, 1998.

9. [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [X ] Power of Attorney

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10. [ ] English translation Document (if applicable)
11. [X] Information Disclosure Statement [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
14. [ ] Small Entity status is claimed.
15. [X] Claim for Convention Priority [ ] Certified copy of Priority Document(s)
    a. Priorities of Japanese application no. 8-183844 filed on July 12, 1996; application no. 8-276634 filed on October 18, 1996; application no. 9-010683 filed on January 23, 1997; and application no. 9-18132 filed on July 7, 1997 is claimed under 35 USC 119. The certified copies have been filed in prior application Serial No. 09/029,608. (For Continuing Applications, if applicable).
16. [ ] Other _____
17. [X] If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

    [ ] Continuation [X] Division [ ] Continuation-in-part (CIP) of prior application no. 09/029,608

    a. [X] Please amend the specification by inserting after the title: --This application is a continuation of prior application Serial No.09/029,608, filed March 15, 1998--.

    b. [X] Cancel in this application original claims 1-86 of the prior application before calculating the filing fee.

| FEE TRANSMITTAL<br>The filing fee is calculated below | Number Filed | Number Extra | Rate | Basic Fee $710.00 |
|---|---|---|---|---|
| Total Claims | 11 - 20 | 0 | x $18.00 | 0 |
| Independent Claims | 8 - 3 | 5 | x $80.00 | 400.00 |
| Multiple Dependent Claims | | | $270.00 | |
| | | | Basic Filing Fee | $710.00 |
| Reduction by 1/2 for small entity | | | | |
| Fee for recording enclosed Assignment | | | $40.00 | |
| TOTAL | | | | $1,110.00 |

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[X] A check in the amount of $1,110.00 is enclosed to cover the filing fee.

[ ] Please charge our Deposit Account No. **01-2340** in the total amount of $710.00 to cover the filing fee and 400.00 extra independent claims. A duplicate of this sheet is attached.

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18. CORRESPONDENCE ADDRESS:

23850

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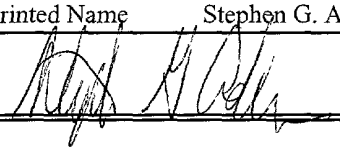
| SUBMITTED BY | | |
|---|---|---|
| Typed or Printed Name | Stephen G. Adrian | Reg. No. 32,878 |
| Signature |  | Date: January 23, 2001 |

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88. A semiconductor device comprising:

a semiconductor element having protruding electrodes formed on a surface thereof, the protruding electrodes having a straight shape on a lateral surface thereof;

a conductive film covering a top surface of the protruding electrodes;

a first resin layer that is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereon; and

a second resin layer provided so as to cover at least a back surface of the semiconductor element.

89. A semiconductor comprising:

a semiconductor element having protruding electrodes formed on a surface thereof, the protruding electrodes having a straight shape on a lateral surface thereof;

a conductive film covering a top surface of the protruding electrodes;

a resin layer which is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; and

external connection protruding electrodes provided to the ends of the protruding electrodes exposed from the resin layer.

90. A semiconductor wafer on which semiconductor elements are provided, comprising:

a semiconductor wafer including a plurality of semiconductor elements having a surface on

95. The semiconductor device as claimed in claim 94, where the protruding electrodes are arranged at an increased pitch than a pitch of the pads.

96. The semiconductor device as claimed in claim 91, wherein the resin layer is formed by disposing a film between the protruding electrodes and a mold, which thus contacts the sealing resin through the film.

97. A semiconductor device comprising:

a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed, the protruding electrodes having a straight shape on a lateral surface thereof;

a conductive film covering a top surface of the protruding electrodes;

lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and

a resin layer which is formed on the surface of the semiconductor element and seals at least a lateral surface of the protruding electrodes;

wherein the lead lines are located between the semiconductor element and the resin layer.

## REMARKS

Claims 87-97 are pending in this application. The above-amendments are made to place the application in better condition for initial examination. Prompt and favorable action on the merits is earnestly solicited.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

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SPECIFICATION

# METHOD AND MOLD FOR MANUFACTURING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, AND METHOD FOR MOUNTING THE DEVICE

## TECHNICAL FIELD

The present invention relates to a method and mold for manufacturing a semiconductor device ,and a semiconductor device, and more particularly to a method and mold for manufacturing a semiconductor device having a chip-size package structure, and such a semiconductor device.

Recently, there has been activity in down-sizing of semiconductor devices and increasing the integration density thereof in order to meet requirements of down-sizing of electronic devices and apparatus. A semiconductor device having a so-called chip-size package structure has been proposed in which the shape of the semiconductor device is arranged so as to be as similar to that of a semiconductor element (chip) as possible.

As an increased number of pins is employed to increase the integration density and the size of the semiconductor device is reduced, external connection terminals are arranged at a reduced pitch. Hence, protruding electrodes (bumps) are used as external connection terminals because a comparatively large number of protection electrodes can be arranged on a reduced space.

## BACKGROUND ART

Fig. 1(A) shows an example of a semiconductor device used for conventional bare chip (flip chip) mounting. A semiconductor device 1 shown in that figure is generally made up of a semiconductor element (semiconductor chip) 2, and a large number of

protruding electrodes (bumps) 4.

The protruding electrodes 4 serving as external connection terminals are arranged, for example, in a matrix formation, on a lower surface of the semiconductor element 2. The protruding electrodes 4 are formed of a soft metal such as solder, and are thus liable to take scratches. Thus, it is difficult to handle and test the protruding electrodes. Similarly, the semiconductor element 2 is in a bare chip formation and is thus liable to take scratches. Thus, it is also difficult to handle and test the semiconductor element 2 as in the case of the protruding electrodes 4.

As shown in Fig. 1(B), the above semiconductor device 1 is mounted on a mount board 5 (for example, a printed wiring board) as follows. First, the protruding electrodes 4 of the semiconductor device 1 are bonded to electrodes 5a formed on the mount board 5. Subsequently, as shown in Fig. 1(C), a so-called under fill resin 6 (indicated by a pear-skin illustration) is provided between the semiconductor element 2 and the mount board 5.

The under fill resin 6 is formed so that a space 7 (approximately equal to the height of the protruding electrodes 4) formed between the semiconductor element 2 and the mount board 5 is filled with a resin having a flowability.

The under fill resin 6 thus formed is provided to prevent occurrence of a break of a bonded portion between the protruding electrodes 4 and the electrodes 5a of the mount board 5 or a bonded portion between the protruding electrodes 4 and the electrodes of the semiconductor element 2 due to stress resulting from a difference in thermal expansion between the semiconductor element 2 and the mount board 5 and stress generated when heat applied at the time of

provide a method and mold for fabricating a semiconductor device and a semiconductor device, and a semiconductor device having an improved efficiency in fabrication and improved reliability.

The present invention has another object to provide a semiconductor device, a method for fabricating the same and a method for mounting the semiconductor device having an increased degree of freedom in layout of terminals and improved reliability.

## DISCLOSURE OF THE INVENTION

The above problems can be solved by the following measures.

A method for fabricating a semiconductor device of the present invention is characterized by comprising: a resin sealing step of loading a substrate on which semiconductor elements having protruding electrodes are formed, and supplying a sealing resin to positions of the protruding electrodes so as to form a resin layer which seals the protruding electrodes and the substrate; a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and a separating step of cutting the substrate together with the resin layer so that the semiconductor elements are separated from each other.

By the resin sealing step, the protruding electrodes which are too delicate to be subjected to a handling test are sealed by the resin layer. The resin layer realizes a surface protection and functions to relax stress generated at interfaces between the electrodes of the semiconductor element and the protruding electrodes. The subsequent protruding electrode exposing step exposes at least ends of the protruding electrodes from the resin layer. When the protruding electrode exposing step is

completed, the protruding electrodes can electrically be connected to an external circuit board or the like. The subsequent separating step cuts the substrate on which the resin layer is formed together with the resin layer, so that the semiconductor elements are separated from each other. Hence, the individual semiconductor chips can be obtained. Since the resin layer is formed in the resin sealing step, it is not required to provide the under fill resin at the time of mounting the semiconductor device. Hence, the mounting operation can easily be carried out. The sealing resin used to form the resin layer is not provided in the narrow space between the semiconductor device and the mounting board, but is provided to the surface of the substrate on which the protruding electrodes are arranged and is thus shaped by molding. Hence, the resin layer can definitely be provided to the entire surface of the substrate on which the protruding electrodes are arranged. Since the resin layer functions to protect all the protruding, it is possible to definitely prevent connections between the protruding electrodes and the electrodes on the mounting board and connections between the protruding electrodes and the electrodes on the semiconductor element from being broken during a heating process. Thus, the reliability of the semiconductor device can be improved.

The above structure may be configured so that the sealing resin used in the resin sealing step has an amount which causes the resin layer to have a height approximately equal to that of the protruding electrodes. Thus, it is possible to prevent excess resin from flowing out from the mold in the resin sealing step and to prevent occurrence of a situation in which the sealing resin is too short to definitely seal the protruding electrodes.

The above method for fabricating the

Hence, it is possible to definitely form the entire surface of the substrate. Hence, all the protruding electrodes formed on the substrate can definitely be sealed by the resin layer. Since the lower mold is made up of a lower mold having a first lower mold half body which is kept stationary and a second lower mold half body which can be elevated with respect to the first lower mold half body, the detachment function can be facilitated, so that the substrate to which the resin layer is formed can be taken out of the mold.

The above method for fabricating the semiconductor device may be configured so that: an excess resin removing mechanism is provided in the mold used in the resin sealing step; and the excess resin removing mechanism removes excess resin and controls a pressure applied to the sealing resin in the mold. Hence, it is possible to easily measure the amount of sealing resin and to precisely seal the protruding electrodes with an appropriate volume. It is also possible to control the pressure applied to the sealing resin in the mold and to thus uniform the pressure during molding. Thus, it is possible to prevent occurrence of babbles in the sealing resin.

The method for fabricating the semiconductor device may be configured so that the resin sealing step uses a sheet-shaped resin as the sealing resin. Hence, the resin layer can definitely be formed on the entire surface of the substrate. Further it is possible to reduce the time it takes the sealing resin to flow from the central portion to the end portion when the sealing resin is placed in the central portion. Hence, the time necessary to complete the resin sealing step can be reduced.

The method for fabricating the semiconductor device may be configured so that the sealing resin is provided to the film before the resin sealing step is executed. Hence, it is possible to perform the film

providing work and the sealing resin filling work at one time, so that the work can efficiently be done.

The method for fabricating the semiconductor device may be configured so that a plurality of sealing resins are provided to the film, and the resin sealing step is continuously carried out while the film is moved. Hence, it is possible to realize automation of the resin sealing step and improve the efficiency in fabricating the semiconductor devices.

The method may be configured so that a reinforcement plate is loaded onto the mold before the substrate is loaded onto the mold in the resin sealing step. Hence, it is possible to prevent the substrate from being deformed due to heat and stress applied in the resin sealing step and to calibrate a warp inherent in the substrate. Hence, the yield can be improved.

The method may be configured so that the reinforcement plate comprises a substance having a heat radiating performance. Hence, the reinforcement plate functions as a heat radiating plate, so that the semiconductor device has improved heat radiating performance.

The method for fabricating the semiconductor device may be configured so that the protruding electrode exposing step uses means for exposing the ends thereof from the resin layer, said means being at least one of a laser beam projection, eximer laser, etching, mechanical polishing, and blasting. When the laser beam projection or eximer laser is used, it is possible to easily and precisely expose the ends of the protruding electrodes. When etching, mechanical polishing or blasting is used, it is possible to expose the ends of the protruding electrodes at low cost.

The method may be configured so that: the film used in the resin sealing step is formed of an

sealing resin formed on the back surface may be formed of resin having performance which can protect the semiconductor element from external force exerted on the semiconductor element.

It is also possible to use, in the resin sealing step, the film having protruding portions located in positions facing the protruding electrodes so that the resin layer is formed in a state in which the protruding portions are pressed against the protruding electrodes. The sealing resin does not adhere to the interfaces between the protruding portions and the protruding electrodes. Hence, by removing the film, the parts of the protruding electrodes (against which the protruding portions are pressed) are exposed from the resin layer. Hence, it is possible to easily and definitely expose the parts of the protruding electrodes from the resin layer.

The protruding electrode exposing step may be configured so that an external connection protruding electrode forming step is executed which forms external connection protruding electrodes on the ends of the protruding electrodes after the ends of the protruding electrodes are exposed from the resin layer. Hence, it is possible to improve the mounting performance at the time of mounting the semiconductor device on the mounting board. That is, the protruding electrodes are formed on the electrodes formed on the semiconductor element, and are necessarily required to be small. Thus, an arrangement in which the small protruding electrodes are used as external connection terminals to be electrically connected to the mounting board has a possibility that the protruding electrodes may not definitely be connected to the mounting board. On the other hand, the external connection protruding electrodes are provided separately from the protruding electrodes formed on the semiconductor element, and can freely be designed so as to be suitable for the

structure of the mounting board. Hence, by forming the external connection protruding electrodes to the ends of the small-size protruding electrodes formed on the semiconductor element, it is possible to improve the mounting performance between the semiconductor device and the mounting board.

The external connection protruding electrode forming step may be configured so that the protruding electrodes and the external connection protruding electrodes are joined by a bonding member having a stress relaxing function. Hence, even if external force is applied to the external connection protruding electrodes, stress caused by the external force is relaxed by the adhesive interposed between the external connection protruding electrodes and the protruding electrodes, so that the stress can be prevented from being transferred to the protruding electrodes. Hence, it is possible to prevent the semiconductor element from being damaged by external stress and to improve the reliability of the semiconductor device.

The method for fabricating the semiconductor device may be configured so that: cutting position grooves are formed, before the resin sealing step is carried out, in the substrate so as to be located in positions in which the substrate is cut in the separating step; and the substrate is cut in the cutting position grooves filled with the sealing resin. Hence, it is possible to prevent a crack from occurring in the substrate and the sealing resin. If the cutting position grooves as defined above are not formed, the separating step cuts the substrate to which the comparatively thing resin layer is formed. In this case, a crack may occur in the resin layer. Further, a large magnitude of stress is applied to the cutting positions, and a crack may occur in the substrate. In contrast, the cutting position grooves

a resin sealing step of arranging the separated semiconductor elements on a base member and sealing a sealing resin so that a resin layer is formed; a protruding electrode exposing step of exposing at least ends of the protruding electrodes from the resin layer; and a second separating step of cutting the resin layer together with the base member in positions between adjacent semiconductor elements, so that the semiconductor elements to which the resin layer is formed are separated from each other. By the first separating step, the substrate on which the semiconductor elements are formed is cut so that individual semiconductor elements can be obtained. In the resin sealing step, the separated semiconductor elements are arranged on the base member. In this case, the semiconductor elements of different types can be mounted on the base member. The semiconductor elements mounted on the base member are sealed by the resin layer of the sealing resin. In the subsequent protruding electrode exposing step, at least the ends of the protruding electrodes are exposed from the resin layer. In the second separating step, the resin layer is cut together with the base member in the boundaries between the adjacent semiconductor elements. Hence, the semiconductor device in which the different semiconductor devices are covered by the same sealing resin. In the second separating step, as in the case of claim 28, it is possible to prevent a crack from occurring in the substrate and the resin layer due to stress generated when cutting.

There is also provided a method for fabricating semiconductor devices characterized by comprising: a resin sealing step of loading a substrate on which semiconductor elements having external connection electrodes formed on surfaces of the semiconductor elements onto a mold and supplying a resin to the surfaces so that a resin layer sealing

the external connection electrodes and the substrate is formed; and a separating step of cutting the substrate together with the resin layer in positions in which the external connection electrodes are formed, so that the semiconductor elements are separated from each other. By the resin sealing step, the external connection electrodes are covered by the resin layer. In the subsequent separating step, the semiconductor elements are separated from each other so that the external connection electrodes are exposed at the interfaces between the substrate and the resin layer in the cut positions. Hence, the external connection electrodes exposed from the side portions of the semiconductor devices can be used to electrically connect the semiconductor devices to the mounting board. The terminal portions can be exposed from the resin layer by merely cutting the substrate in the position in which the external connection electrodes are formed. Hence, the semiconductor devices can be produced very easily.

The method may be configured so that the external connection electrodes are commonly owned by adjacent ones of the semiconductor elements before the separating step is executed. Hence, by preforming the step only one time, two semiconductor devices can be provided so that the separated external connection electrodes are exposed. Hence, the semiconductor devices can efficiently be fabricated. In addition, it is possible to suppress occurrence of unwanted portions on the substrate and to efficiently utilize the substrate.

The method for fabricating the semiconductor device may be configured so that positioning grooves are formed on a back surface of the resin layer or the substrate after the resin sealing step is executed and before the separating step is executed. For example, when the semiconductor devices thus fabricated are

substrate is fixed to the first lower mold half body, and it is thus possible to prevent occurrence of a deformation in the substrate such as a warp and to calibrate a warp inherent in the substrate. When the attachment/detachment mechanism performs the detachment operation, the substrate is urged toward the detaching direction from the first lower mold half body. Hence the detachability of the substrate from the mold can be improved.

The attachment/detachment mechanism may comprise: a porous member arranged in the position of the first lower mold half body onto which the substrate is loaded; and an intake/exhaust device preforming a gas suction and supply process for the porous member. The porous member is supplied with a gas from an intake/exhaust apparatus, and injects the gas towards the substrate. When the gas is injected towards the substrate through the porous member at the time of detaching the substrate from the mold, the detachability of the substrate from the mold can be improved. When the intake/exhaust apparatus performs the sucking process, the substrate is sucked towards the porous member. Hence, it is possible to prevent occurrence of a deformation of the substrate such as a warp and to calibrate a warp inherent in the substrate. Since the porous member is disposed to the position on the first lower mold half body, the porous member is covered by the substrate in the sealing resin is supplied in the resin sealing step. Hence, the sealing resin cannot enter the porous member. In addition, the back surface of the substrate is directly urged along the detaching direction at the time of detaching the substrate from the mold, the detachability can be improved.

The mold may be configured so that an area enclosed by the second lower mold half body is wider than an area of an upper portion of the first lower

mold half body in a state in which the cavity is formed. Hence, the detachability can be moved, and a rectangular step portion can easily be defined by the above arrangement.

There is provided a semiconductor device characterized by comprising: a semiconductor element having a surface on which protruding electrodes are directly formed; and a resin layer which is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof. The resin layer functions to protect the semiconductor element, the protruding electrodes, the mounting board and the connections therebetween. Since the resin layer is already formed in the semiconductor device before the mounting step, it is not required to perform the conventional process for providing under fill resin at the time of mounting the semiconductor device to the mounting board, so that the mounting process can easily be performed.

The semiconductor device may be configured so that there is provided a heat radiating member provided on a back surface of the semiconductor element opposite to the surface thereof on which the protruding electrodes are provided. Hence, it is possible to improve the heat radiating performance of the semiconductor device and improve the strength thereof.

There is also provided a semiconductor device characterized by comprising: a semiconductor element having a surface on which external connection electrodes are provided which are to be electrically connected to external terminals; and a resin layer provided on the surface of the semiconductor element so as to cover the external connection electrodes, wherein the external connection electrodes are laterally exposed at an interface between the semiconductor element and the resin layer. Hence, the

substrate because the semiconductor element and the sealing resin have different thermal expansion ratios and a warp may occur in the semiconductor element. In contrast, according to the above structure, the front and back surfaces of the substrate are covered by the respective resin layers and so that the states of the front and back surfaces of the substrate can be equalized and the semiconductor device can be well balanced. Hence, it is possible to prevent occurrence of a warp in the semiconductor device during the thermal process. The sealing resin provided to the lower surface of the semiconductor element has a characteristic different from that of the sealing resin provided to the upper surface thereof. For example, the sealing resin formed on the front surface on which the protruding electrodes are arranged may be formed of resin having performance which can relax stress applied to the protruding electrodes. The sealing resin formed on the back surface may be formed of resin having performance which can protect the semiconductor element from external force exerted on the semiconductor element.

There is also provided a semiconductor device characterized by comprising: a semiconductor element having protruding electrodes formed on a surface thereof; a resin layer which is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; and external connection protruding electrodes provided to the ends of the protruding electrodes exposed from the resin layer. Hence, it is possible to improve the mounting performance at the time of mounting the semiconductor device on the mounting board. That is, the protruding electrodes are formed on the electrodes formed on the semiconductor element, and are necessarily required to be small. Thus, an

and those of the mounting board can easily be established.

The above-mentioned structures of the present invention correspond to first through twenty ninth embodiments (Figs. 1 through 77) of the present invention, which will be described later.

The following structures of the present invention correspond to thirtieth through fifty third embodiments (Figs. 1 through 117E), which will be described later.

There is provided a method for fabricating a semiconductor device comprising: a resin sealing step of loading a wiring board having a flexible member on which a semiconductor element and leads are arranged onto a mold and supplying sealing resin to the semiconductor element so as to seal the semiconductor element; and a protruding electrode forming step of forming protruding electrodes so as to be electrically connected to the leads formed on the wiring board, the resin sealing step uses a compression-molding process. In the resin sealing step, the wiring board is loaded onto the mold, and the semiconductor element is sealed by the sealing resin. In the protruding electrode forming step, the protruding electrodes are formed so as to be electrically connected to the leads formed on the wiring board. A compression molding method is used as means for sealing the semiconductor element in the resin sealing step. Hence, it is possible to definitely provide the resin to a narrow gap between the semiconductor element and the wiring board. Since the compression-molding process uses a comparatively low forming pressure, it is possible to prevent, in the resin molding step, the substrate from being deformed and prevent a load from being applied to electrical connections between the semiconductor elements and the wiring board. Hence, it is possible to the connection between the semiconductor element

semiconductor element is placed; and a bending step of bending the extending portions is executed after the resin sealing step is completed and before the protruding electrode forming step is executed. The method may also be configured so that: extending portions are formed to the wiring board so that the extending portions laterally extend from a position in which the semiconductor element is placed; a bending step of bending the extending portions is carried out before the resin sealing step is executed; and the resin sealing step and the protruding electrode forming step are carried out after the bending step is executed. Thus, a comparatively wide area for the formation of the protruding electrodes. Hence, it is possible to increase the arrangement pitch for the protruding electrodes and to arrange an increased number of protruding electrodes. The bending step may be executed before or after the resin sealing step.

The method for fabricating the semiconductor device may be configured so that: connection electrodes to be connected to the semiconductor element are formed to ends of the extending portions; and an element connecting step of connecting the semiconductor element and the connection electrodes is executed after the bending step is carried out. Since the semiconductor element and the connection electrodes are not yet connected at the time of binding the extending portions, the reliability of the connections between the semiconductor element and the connection electrodes can be improved.

The method for fabricating the semiconductor device may be configured so that the connection electrodes are arranged in an interdigital formation, and have curved corners. Hence, it is possible to increase the areas of the connection electrodes and to thus simplify the process for making connections with the semiconductor element. When the connections

between the semiconductor element and the connection electrodes are made by a wire bonding method, stress generated when a bonding tool (ultrasonic welding tool) touches the connection electrodes can be decentralized because the corner portions of the connection electrodes are curved. Hence the process for electrically connecting the semiconductor element and the connection electrodes can definitely be carried out.

There is also provided a semiconductor device characterized by comprising: a semiconductor element; protruding electrodes functioning as external connection terminals; a wiring board having a flexible base on which leads are formed, the leads having ends connected to the semiconductor element and other ends connected to the protruding electrodes; and a sealing resin sealing the semiconductor element, there are provided extending portions that are formed to the wiring board so that the extending portions laterally extend from a position in which the semiconductor element is placed, the protruding electrodes being formed on the extending portions. A comparatively wide area can be obtained for forming the protruding electrodes. Hence, it is possible to increase the arrangement pitch for the protruding electrodes or arrange an increased number of protruding electrodes. The bending step may be carried out before or after the resin sealing step.

The semiconductor device may be configured so that there is provided a frame which supports the wiring board and has a cavity which accommodates the semiconductor element. Hence, the flexible wiring board can be supported by the frame and thus the semiconductor element can also be supported thereby.

The semiconductor device may be configured so that the protruding electrodes are mechanical bumps obtained by plastic-deforming the leads. The bumps

characterized by comprising: a mounting member including connection pins that are flexibly deformable and are located in positions corresponding to those of the external connection terminals, and a positioning member positioning the connection pins, upper ends of the connection pins being connected to the external connection terminals of the semiconductor device, and lower ends thereof being connected to the mounting board. Hence, the connection pins are interposed between the external connection terminals and the mounting board. The connection pins are flexible, and are capable of absorbing stress due to a difference in thermal expansion coefficient between the semiconductor device and the mounting board during a thermal process. Hence, the connections between the external connection terminals and the mounting board can definitely be maintained irrespective of the stress, so that the reliability of mounting can be improved. The connection pins are positioned by the positioning member so as to be located in positions corresponding to those of the external connection terminals. Hence, it is not required to position the individual connection pins and the external connection terminals or the mounting board, so that the mounting operation can easily be carried out.

There is also provided a semiconductor device characterized by comprising: a semiconductor device main body having a semiconductor element having a surface on which protruding electrodes are directly formed, and a resin layer which is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; an interposer to which the semiconductor device main body is attached, a wiring pattern to which the semiconductor device main body is connected being formed on a base member of the interposer; an anisotropic conductive film which has an adhesiveness

and a conductivity in a pressed direction and is interposed between the semiconductor device main body and the interposer, the anisotropic conductive film fixing the semiconductor device main body to the interposer and electrically connecting them; and external connection terminals which are connected to the wiring pattern through holes formed in the base member and are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided. Thus, the resin layer protects the semiconductor element and the protruding electrodes, and also functions as an under fill resin. Further, the semiconductor device main body is attached to the interposer, and the wiring pattern is formed on the base member. Hence, the wiring pattern can arbitrarily be formed on the base member. The external connection terminals are connected to the wiring pattern via the holes formed in the base member. Since the wiring pattern can arbitrarily be set, the external connection terminals can be determined independently of the positions of the protruding electrodes provided on the semiconductor device main body. Hence, the degree of freedom in layout of the external connection terminals can be increased. Further, since the anisotropic conductive film has an adhesiveness and a conductivity in the pressing direction, the semiconductor device main body and the interposer can be connected by the anisotropic terminals. The adhesiveness of the anisotropic conductive film mechanically bonds the semiconductor device main body and the interposer, and the anisotropic conductivity electrically bonds (connects) them. As described above, the anisotropic conductive film has both the adhesiveness and the conductivity, it is possible to reduce the number of components and the number of assembly steps, as compared to an

arrangement in which the adhesiveness and the conductivity are implemented by respective members. Further, the anisotropic conductive film has flexibility, and is provided between the semiconductor device main body and the interposer. Hence, the anisotropic conductive film functions as a buffer film. Hence, the anisotropic conductive film is capable of relaxing stress generated between the semiconductor device main body and the interposer.

The semiconductor device may be configured so that an arrangement pitch for the protruding electrodes provided on the semiconductor device main body is equal to that for the external connection terminals provided on the interposer. Hence, the size of the interposer can be reduced, and the semiconductor device can be down sized.

The semiconductor device may be configured so that an arrangement pitch for the external connection terminals provided on the interposer is greater than that for the protruding electrodes provided on the semiconductor device. Hence, the degree of freedom in routing the wiring pattern on the interposer can be improved.

The semiconductor device may be configured so that there is provided an insulating member which is provided on the interposer and has holes located in positions facing the protruding electrodes. Hence, the pressing pressure applied when the semiconductor device main body is attached to the interposer concentrates on the holes. Thus, the conductivity at the holes can be enhanced, and thus the semiconductor device main body and the interposer can definitely be connected.

The semiconductor device may be configured so that the interposer comprises a TAB (Tape Automated Bonding) tape. The TAB tape is available as a component of the semiconductor devices at low cost.

Hence, the use of the TAB tape contributes to reducing the cost.

There is also provided a method for fabricating a semiconductor device, characterized by comprising: a semiconductor device main body forming step of forming a semiconductor device main body having a semiconductor element having a surface on which protruding electrodes are directly formed, and a resin layer which is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; an interposer forming step of forming an interposer to which the semiconductor device main body is attached, a wiring pattern to which the semiconductor device main body is connected being formed on a base member of the interposer; a bonding step of bonding the semiconductor device main body and the interposer by an anisotropic conductive film which has an adhesiveness and a conductivity in a pressed direction, the anisotropic conductive film fixing the semiconductor device main body to the interposer and electrically connecting them; and an external connection terminal forming step of forming external connection terminals which are connected to the wiring pattern through holes formed in the base member and are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided. Since the resin layer is provided to the surface of the semiconductor device main body so that the ends thereof remain, the resin layer protects the semiconductor element and the protruding electrodes, and functions as an under fill resin. The semiconductor device main body is attached to the interposer, and the wiring pattern to which the semiconductor device main body is connected is formed on the base member. Hence, the wiring pattern can arbitrarily be formed on the base member. The

a wiring pattern to which the semiconductor device main body is connected being formed on a base member of the interposer; an adhesive which is provided between the semiconductor device main body and the interposer and which bonds the semiconductor device main body to the interposer; a conductive member which electrically connects the semiconductor device main body and the interposer; and external connection terminals which are connected to the wiring pattern through holes formed in the base member and are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided. Since the resin layer is provided to the surface of the semiconductor device main body so that the ends thereof remain, the resin layer protects the semiconductor element and the protruding electrodes, and functions as an under fill resin. The semiconductor device main body is attached to the interposer, and the wiring pattern to which the semiconductor device main body is connected is formed on the base member. Hence, the wiring pattern can arbitrarily be formed on the base member. The external connection terminals are connected to the wiring pattern via the holes formed in the base member. Since the wiring pattern can arbitrarily be set, the external connection terminals can be determined independently of the positions of the protruding electrodes provided on the semiconductor device main body. Hence, the degree of freedom in layout of the external connection terminals can be increased. Further, the adhesive mechanically bonds the semiconductor device main body and the interposer, and the conductive member electrically bonds (connects) the semiconductor device main body and the interposer. As described above, the mechanical bonding and electrical bonding can separately be implemented by the respective members, so that

substances respectively optimal to implementation of the functions (the mechanical bonding function and electrical bonding function) can be selected. Hence, the mechanical and electrical connections between the semiconductor device main body and the interposer can definitely be realized, and the reliability of the semiconductor device can be improved.

The adhesive has a given flexibility after it is hardened, and is provided between the semiconductor device main body and the interposer. Hence, the adhesive functions as a buffer film, and relaxes stress generated between the semiconductor device main body and the interposer.

The semiconductor device may be configured so that the conductive member is a conductive paste. Hence, a conductive member can be provided merely by coating the protruding electrodes or the wiring pattern of the interposer with the conductive paste. Thus, the work of assembling the semiconductor device can easily be performed. The conductive paste can be coated by a known transfer method or printing method, so that the conductive member can efficiently be provided.

The semiconductor device may be configured so that the conductive member comprises stud bumps. Hence, the protruding electrodes of the semiconductor element and the wiring pattern of the interposer can be connected through the stud bumps, so that electrical connections can definitely be made.

The semiconductor device may be configured so that the conductive member comprises flying leads, which are integrally formed with the wiring pattern and bypasses the adhesive so as to be connected to the protruding electrodes. Hence, there is no adhesive provided to the contacts between the flying leads and the protruding electrodes, and the reliability thereof can be improved. The flying leads have a spring

member. Thus, even if the connection pins are deformed, the positioning member is capable of following the above deformation and thus absorbing stress generated between the semiconductor device main body and the interposer.

There is also provided a method for fabricating a semiconductor device, characterized by comprising: a semiconductor device main body forming step of forming a semiconductor device main body having a semiconductor element having a surface on which protruding electrodes are directly formed, and a resin layer which is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; an interposer forming step of forming an interposer to which the semiconductor device main body is attached, a wiring pattern to which the semiconductor device main body is connected being formed on a base member of the interposer; a conductive member arranging step of arranging a conductive member to at least one of the semiconductor device main body and the interposer; a bonding step of bonding the semiconductor device main body and the interposer by an adhesive and connecting them electrically; and an external connection terminal forming step of forming external connection terminals which are connected to the wiring pattern through holes formed in the base member and are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided. Since the resin layer is provided to the surface of the semiconductor device main body so that the ends thereof remain, the resin layer protects the semiconductor element and the protruding electrodes, and functions as an under fill resin. The semiconductor device main body is attached to the interposer, and the wiring pattern to which the semiconductor device main body is connected is formed

on the base member. Hence, the wiring pattern can arbitrarily be formed on the base member. The external connection terminals are connected to the wiring pattern via the holes formed in the base member. Since the wiring pattern can arbitrarily be set, the external connection terminals can be determined independently of the positions of the protruding electrodes provided on the semiconductor device main body. Hence, the degree of freedom in layout of the external connection terminals can be increased. Further, the adhesive mechanically bonds the semiconductor device main body and the interposer, and the conductive member electrically bonds (connects) the semiconductor device main body and the interposer. As described above, the mechanical bonding and electrical bonding can separately be implemented by the respective members, so that substances respectively optimal to implementation of the functions (the mechanical bonding function and electrical bonding function) can be selected. Hence, the mechanical and electrical connections between the semiconductor device main body and the interposer can definitely be realized, and the reliability of the semiconductor device can be improved.



BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram of a resin sealing step of a method for fabricating a semiconductor device according to a first embodiment of the present invention and a mold for fabricating a semiconductor device according to the first embodiment of the present invention. Figs. 1A - 1C are diagrams showing a conventional semiconductor device and its fabrication method.

Fig. 2 is a diagram showing the resin sealing step in the method for fabricating the semiconductor device according to the first embodiment

of the present invention.

Fig. 3 is another diagram showing the resin sealing step in the method for fabricating the semiconductor device according to the first embodiment of the present invention.

Fig. 4 is yet another diagram showing the resin sealing step in the method for fabricating the semiconductor device according to the first embodiment of the present invention.

Fig. 5 is a further diagram showing the resin sealing step in the method for fabricating the semiconductor device according to the first embodiment of the present invention.

Fig. 6 is a diagram showing a protruding electrode exposing step in the method for fabricating the semiconductor device according to the first embodiment of the present invention, wherein (A) shows a substrate observed immediately after the resin sealing step is completed, and (B) is a diagram of an enlarged view of a part indicated by arrow A in (A).

Fig. 7 is another diagram showing the protruding electrode exposing step in the method for fabricating the semiconductor device according to the first embodiment of the present invention, wherein (A) shows the substrate observed when a film is flaking off, and (B) is a diagram of an enlarged view of a part indicated by arrow B in (B).

Fig. 8 is a diagram showing a separating step in the method for fabricating the semiconductor device according to the first embodiment of the present invention.

Fig. 9 is a diagram showing a semiconductor device according to the first embodiment of the present invention.

Fig. 10 is a diagram showing a method for fabricating a semiconductor device according to a second embodiment of the present invention and a mold

(B).

Fig. 21 is yet another diagram showing the method for fabricating a semiconductor device according to the seventh embodiment of the present invention.

Fig. 22 is a diagram showing a mold for fabricating a semiconductor device according to a third embodiment of the present invention.

Fig. 23 is a diagram showing a mold for fabricating a semiconductor device according to a fourth embodiment of the present invention.

Fig. 24 is a diagram showing a mold for fabricating a semiconductor device according to a fifth embodiment of the present invention.

Fig. 25 is a diagram showing a mold for fabricating a semiconductor device according to a sixth embodiment of the present invention.

Fig. 26 is a diagram showing a semiconductor device according to a second embodiment of the present invention.

Fig. 27 is a diagram showing a semiconductor device according to a third embodiment of the present invention.

Fig. 28 is a diagram showing a method for fabricating a semiconductor device according to an eighth embodiment of the present invention.

Fig. 29 is a diagram showing a method for fabricating a semiconductor device according to a ninth embodiment of the present invention.

Fig. 30 is a diagram showing a method for fabricating a semiconductor device according to a tenth second embodiment of the present invention.

Fig. 31 is a diagram showing a method for fabricating a semiconductor device according to an eleventh embodiment of the present invention.

Fig. 32 is a diagram (part 1) showing a method for fabricating a semiconductor device

embodiment of the present invention.

Fig. 58 is a diagram showing a method for mounting a semiconductor device according to a seventh embodiment of the present invention.

Fig. 59 is a diagram showing a method for fabricating a semiconductor device according to a twenty eighth embodiment of the present invention.

Fig. 60 is a diagram (part 1) showing a method for fabricating a semiconductor device according to a twenty ninth embodiment of the present invention.

Fig. 61 is another diagram (part 2) showing the method for fabricating a semiconductor device according to the twenty ninth embodiment of the present invention.

Fig. 62 is yet another diagram (part 3) showing the method for fabricating a semiconductor device according to the twenty ninth embodiment of the present invention.

Fig. 63 is a diagram showing a semiconductor device according to a fourth embodiment of the present invention.

Fig. 64 is a diagram showing a method for mounting a semiconductor device according to an eighth embodiment of the present invention.

Fig. 65 is a diagram showing a method for mounting a semiconductor device according to a ninth embodiment of the present invention.

Fig. 66 is a diagram showing a method for mounting a semiconductor device according to a tenth embodiment of the present invention.

Fig. 67 is a diagram showing a method for mounting a semiconductor device according to an eleventh embodiment of the present invention.

Fig. 68 is a diagram (part 1) showing another method for mounting a semiconductor device.

Fig. 69 is a diagram (part 2) showing

another method for mounting a semiconductor device.

Fig. 70 is a diagram (part 3) showing another method for mounting a semiconductor device.

Fig. 71 is a diagram showing another semiconductor device.

Fig. 72 is a diagram (part 1) showing yet another method for mounting a semiconductor device.

Fig. 73 is a diagram (part 2) showing yet another method for mounting a semiconductor device.

Fig. 74 is a diagram (part 3) showing yet another method for mounting a semiconductor device.

Fig. 75 is a diagram (part 4) showing yet another method for mounting a semiconductor device.

Fig. 76 is a diagram showing a variation of the mold for fabricating a semiconductor device according to the sixth embodiment of the present invention.

Fig. 77 is a diagram showing another variation of the mold for fabricating a semiconductor device according to the sixth embodiment of the present invention.

Fig. 78 is a diagram showing a semiconductor device according to a thirtieth embodiment of the present invention.

Fig. 79 is a diagram (part 1) showing a method for fabricating the semiconductor device according to the thirtieth embodiment of the present invention.

Fig. 80 is a diagram (part 2) showing a method for fabricating the semiconductor device according to the thirtieth embodiment of the present invention.

Fig. 81 is a diagram showing a semiconductor device according to a thirty first embodiment of the present invention.

Fig. 82 is a diagram (part 1) showing a method for fabricating the semiconductor device

according to the thirty first embodiment of the present invention.

Fig. 83 is a diagram (part 2) showing a method for fabricating the semiconductor device according to the thirty first embodiment of the present invention.

Fig. 84 is a diagram showing a semiconductor device according to a thirty second embodiment of the present invention.

Fig. 85 is a diagram showing a semiconductor device according to a thirty third embodiment of the present invention.

Fig. 86 is a diagram showing a semiconductor device according to a thirty fourth embodiment of the present invention.

Fig. 87 is a diagram showing an excess resin removing mechanism.

Fig. 88 is a diagram showing a semiconductor device according to a thirty fifth embodiment of the present invention.

Fig. 89 is a diagram (part 1) showing a method for fabricating the semiconductor device according to the thirty fifth embodiment of the present invention.

Fig. 90 is a diagram (part 2) showing a method for fabricating the semiconductor device according to the thirty fifth embodiment of the present invention.

Fig. 91 is a diagram showing a semiconductor device and its fabrication method according to a thirty sixth embodiment of the present invention.

Fig. 92 is a diagram showing a semiconductor device and its fabrication method according to a thirty seventh embodiment of the present invention.

Fig. 93 is a diagram showing a semiconductor device and its fabrication method according to a thirty eighth embodiment of the present invention.

Fig. 94 is a diagram showing a semiconductor device and its fabrication method according to a thirty ninth embodiment of the present invention.

Fig. 95 is a diagram showing a semiconductor device and its fabrication method according to a fortieth embodiment of the present invention.

Fig. 96 is a diagram showing a semiconductor device and its fabrication method according to a forty first embodiment of the present invention.

Fig. 97 is a diagram showing a semiconductor device and its fabrication method according to a forty second embodiment of the present invention.

Fig. 98 is a diagram showing a semiconductor device and its fabrication method according to a forty third embodiment of the present invention.

Fig. 99 is a diagram showing a semiconductor device and its fabrication method according to a forty fourth embodiment of the present invention.

Fig. 100 is a diagram showing a semiconductor device and its fabrication method according to a forty fifth embodiment of the present invention.

Fig. 101 is a diagram showing a semiconductor device and its fabrication method according to a forty sixth embodiment of the present invention.

Fig. 102 is a diagram showing a semiconductor device and its fabrication method according to a forty seventh embodiment of the present invention.

Fig. 103 is a diagram showing another embodiment of a wiring board (part 1).

Fig. 104 is a diagram showing yet another embodiment of a wiring board (part 2).

Fig. 105 is a diagram showing a further embodiment of a wiring board (part 3).

Fig. 106 is a diagram showing a still

further embodiment of a wiring board (part 4).

Fig. 107 is a diagram showing yet another embodiment of a wiring board (part 5).

Fig. 108 is a diagram showing another embodiment of a wiring board (part 6).

Fig. 109 is a diagram showing a further embodiment of a wiring board (part 7.

Fig. 110 is a diagram showing a variation of the wiring board shown in Fig. 106.

Fig. 111 is a diagram showing a semiconductor device according to a forty eighth embodiment of the present invention.

Fig. 112 is a diagram (part 1) showing a method for fabricating the semiconductor device according to the forty eighth embodiment of the present invention.

Fig. 113 is a diagram (part 2) showing a method for fabricating the semiconductor device according to the forty eighth embodiment of the present invention.

Fig. 114 is a diagram showing a semiconductor device and its fabrication method according to a forty ninth embodiment of the present invention.

Fig. 115 is a diagram showing a semiconductor device and its fabrication method according to a fiftieth embodiment of the present invention.

Fig. 116 is a diagram showing semiconductor devices according to fifty first through fifty third embodiments of the present invention.

Fig. 117 is a diagram showing various semiconductor devices to which mechanical bumps are applied.

Fig. 118 is a diagram showing a semiconductor device according to a fifth fourth embodiment of the present invention.

Fig. 119 is a diagram (part 1) showing a method for fabricating the semiconductor device according to the fifty fourth embodiment of the present invention.

Fig. 120 is a diagram (part 2) showing a method for fabricating the semiconductor device according to the fifty fourth embodiment of the present invention.

Fig. 121 is a diagram (part 3) showing a method for fabricating the semiconductor device according to the fifty fourth embodiment of the present invention.

Fig. 122 is a diagram (part 4) showing a method for fabricating the semiconductor device according to the fifty fourth embodiment of the present invention.

Fig. 123 is a diagram showing a semiconductor device according to a fifty fifth embodiment of the present invention.

Fig. 124 is a diagram showing a semiconductor device according to a fifty sixth embodiment of the present invention.

Fig. 125 is a diagram showing a semiconductor device according to a fifty seventh embodiment of the present invention.

Fig. 126 is a diagram (part 1) showing a method for fabricating the semiconductor device according to the fifty fifth embodiment of the present invention.

Fig. 127 is a diagram (part 2) showing a method for fabricating the semiconductor device according to the fifty fifth embodiment of the present invention.

Fig. 128 is a diagram showing a mounting arrangement for a semiconductor device according to a fifty fourth embodiment of the present invention.

Fig. 129 is a diagram showing a mounting

arrangement for a semiconductor device according to a fifty fifth embodiment of the present invention.

Fig. 130 is a diagram showing a mounting arrangement for a semiconductor device according to a fifty sixth embodiment of the present invention.

Fig. 131 is a diagram showing a mounting arrangement for a semiconductor device according to a fifty seventh embodiment of the present invention.

Fig. 132 is a diagram showing a mounting arrangement for a semiconductor device according to a fifty eighth embodiment of the present invention.

Fig. 133 is a diagram showing a mounting arrangement for a semiconductor device according to a fifty ninth embodiment of the present invention.

Fig. 134 is a diagram showing a mounting arrangement for a semiconductor device according to a sixtieth embodiment of the present invention.

Fig. 135 is a diagram showing a semiconductor device according to a fifth seventh embodiment of the present invention.

Fig. 136 is a diagram (part 1) showing a method for fabricating a semiconductor device according to a fifty sixth embodiment of the present invention.

Fig. 137 is a diagram (part 2) showing a method for fabricating the semiconductor device according to the fifty sixth embodiment of the present invention.

Fig. 138 is a diagram (part 3) showing a method for fabricating the semiconductor device according to the fifty sixth embodiment of the present invention.

Fig. 139 is a diagram (part 4) showing a method for fabricating the semiconductor device according to the fifty sixth embodiment of the present invention.

Fig. 140 is a diagram (part 5) showing a

method for fabricating the semiconductor device according to the fifty sixth embodiment of the present invention.

Fig. 141 is a diagram (part 6) showing a method for fabricating the semiconductor device according to the fifty sixth embodiment of the present invention.

Fig. 142 is a diagram showing a semiconductor device according to a fifty ninth embodiment of the present invention.

Fig. 143 is a diagram showing a semiconductor device according to a sixtieth embodiment of the present invention.

Fig. 144 is a diagram showing a semiconductor device according to a sixty first embodiment of the present invention.

Fig. 145 is a diagram showing a semiconductor device according to a sixty second embodiment of the present invention.

Fig. 146 is a diagram showing a semiconductor device according to a sixty third embodiment of the present invention.

Fig. 147 is a diagram showing a semiconductor device according to a sixty fourth embodiment of the present invention.

Fig. 148 is a diagram showing a method for fabricating a semiconductor device according to a fifty seventh embodiment of the present invention.

Fig. 149 is a diagram showing a semiconductor device according to a sixty fifth embodiment of the present invention.

Fig. 150 is a diagram showing a method for fabricating a semiconductor device according to a fifty eighth embodiment of the present invention (part 1).

Fig. 151 is a diagram showing a method for fabricating a semiconductor device according to the

bumps 12 are arranged on a mount surface of the semiconductor substrate. The bumps 12 are provided by, for example, arranging semiconductor balls on the mount surface by a transfer method, and function as external connection electrodes. In the present embodiment, the bumps 12 are provided directly on electrode pads (not shown) formed on the semiconductor element 11.

The resin layer 13 (indicated by a pear-skin illustration) is formed of, for example, thermosetting resin such as polyimide and epoxy resin (PPS, PEK, PES and thermoplastic resin such as heat-resistant liquid crystal resin), and is provided on the whole bump formation surface of the semiconductor element 11. Hence, the bumps 12 arranged on the semiconductor element 11 are sealed by the resin layer 13 so that ends of the bumps 12 are exposed from the resin layer 13. That is, the resin layer 13 is provided to the semiconductor element 11 so as to seal the bumps 12 except for the ends thereof.

The semiconductor device 10 having the above structure has a chip-size package structure in which the whole size thereof is approximately equal to the size of the semiconductor chip 11. Hence, the semiconductor 10 sufficiently meets a recent requirement for down sizing.

As described above, the semiconductor device 10 has the resin layer 13 which is provided on the semiconductor element 11 and seals the bumps 12 so that the ends thereof are exposed. Hence, the bumps 12 which are liable to take scratches are protected by the resin layer 13, which thus has the same function as the under fill resin 6 conventionally used (see Fig. 78).

That is, it is possible to prevent occurrence of a break of the bonded portions between the semiconductor element 11, the bumps 12, a mount

The upper mold 21 can be elevated in directions Z1 and Z2 indicated by an arrow by means of an elevating apparatus that is not shown. The lower surface of the upper mold 21 is a cavity surface 21a, which is flat. The upper mold 21 has a very simple shape, which can be produced at a less-expensive cost.

The lower mold 22 is made up of a first lower mold half body 23 and a second lower mold half body 24. The first lower mold half body 23 has a shape that corresponds to the shape of the substrate 16, and is, more particularly, slightly greater than the substrate 16. The substrate 16 is loaded onto a cavity surface 25 formed on the upper surface of the first lower mold half body 23.

The second lower mold half body 24 has an approximately ring shape which surrounds the first lower mold half body 23. The second lower mold half body 24 can be elevated in the directions indicated by the arrows Z1 and Z2 by means of an elevating apparatus which is not shown. The second lower mold half body 24 has an inner peripheral wall which defines a cavity surface 26. A slant surface 27 facilitating a mold detaching step is formed in a given upper range of the cavity surface 26.

In the state immediately after the resin sealing step is started, as shown in Fig. 1, the second lower mold half body 24 is located above the first lower mold half body 23 in the direction Z2. Hence, the substrate 16 can be placed in a recess (cavity) defined by the first and second mold half bodies 23 and 24. The substrate 16 is loaded so that the surface on which the bumps 12 are provided faces upwards. Hence, the bumps 12 on the substrate 16 in the loaded state face the upper mold 21.

After the substrate 16 is loaded onto the lower mold 22, a film 30 is provided below the upper mold 21 so that it does not have any deformation.

generated by the compression molding will be increased to a level which may damage the bumps 12. If the upper mold 21 and the second lower mold half body 24 move at a relatively low speed, the efficiency in fabrication will be degraded. With the above in mind, the moving speed of the upper mold 21 and the second lower mold half body 24 is selected to an appropriate value at which the above two problems do not occur.

The upper mold 21 and the second lower mold half body 24 move down until the film 30 clamped comes into contact with the bumps 12 with pressure. In the state in which the film 30 contacts the bumps 20 with a pressure, the sealing resin 35 seals all the bumps 12 and the substrate 16. Fig. 4 shows a state in which the resin layer forming step is completed. In this state, the film 30 is urged towards the substrate 16 and is in contact therewith with a pressure. Hence, the ends of the bumps 12 fall in the film 30. Further, the sealing resin 35 is provided on the entire surface of the substrate 16, so that the resin layer 13 sealing the bumps 12 is formed.

The amount of resin of the resin layer 35 is obtained beforehand so that the resin layer 13 has a height approximately equal to that of the bumps 12 when the resin layer forming step is completed. By selecting an appropriate amount of resin beforehand, it is possible to prevent excessive resin from flowing out of the mold 20 and prevent occurrence of incomplete sealing of the bumps 12 and the substrate 16 by an insufficient amount of resin.

The resin layer forming step is followed by the mold detaching step. The mold detaching step commences moving up the upper mold 21 in the direction Z2. The resin layer 13 is fixed to the slant portion 27 of the second lower mold half body 24. Hence, the substrate 16 and the resin layer 13 are retained in the lower mold 22. Hence, only upper mold 21 is

16 to which the resin layer 13 is provided can definitely be detached from the first lower mold half body 23.

As described above, the resin layer 13 is compression-molded by the mold 20 in the resin layer forming step. In addition, the sealing resin 35 from which the resin layer 13 is formed is not provided between the conventional narrow space between the semiconductor device 1 and the mount board 5 (see Fig. 78). That is, the sealing resin 35 is mounted on the surface of the substrate 16 on which the bumps 12 are arranged, and is then molded.

Hence, the resin layer 13 can definitely be provided on the whole surface of the substrate 16 on which the bumps 12 are formed, and can definitely be provided in a narrow space having a height approximately equal to the height of the bumps 12. Hence, all the bumps 12 formed on the substrate 16 can definitely be sealed by the resin layer 13, which thus supports the all the bumps 12. Hence, at the time of applying heat as described with reference to Fig. 9, it is possible to definitely prevent occurrence of a break of a bonded portion between the bumps 12 and the mount board 14 and improve the reliability of the semiconductor device 10.

As described previously, the lower mold 22 of the mold 20 is made up of the fixed first lower mold half body 23 and the second lower mold half body 24 that can be elevated with respect to the first lower mold half body 23. Hence, by elevating the second lower mold half body 24 with respect to the first lower mold half body 23 after the resin layer 13 is formed, the substrate 16 to which the resin layer 13 is provided can easily be taken out of the mold 20.

After the above resin sealing step, the protruding electrode exposing step is carried out. Figs. 6 and 7 show the protruding electrode exposing

step. When the resin sealing step is completed, as shown in Fig. 6, the film 30 is fixed to the resin layer 13. Since the film 30 is made of an elastic material, the ends of the bumps 12 fall in the film 30 through the resin layer 13. That is, the ends of the bumps 12 are not covered by the resin layer 13 (this state is enlarged in Fig. 6(B)).

In the protruding electrode exposing step of the present embodiment, as shown in Fig. 7(A), the film 30 is detached from the resin layer 13. Hence, as shown in Fig. 7(B), the ends of the bumps 12 are exposed from the resin 13, and the mounting step can be carried out by using the exposed ends of the bumps 12.

As described above, the protruding electrode exposing step of the present embodiment is a simple process of merely detaching the film 30 from the resin layer 13, and can be executed efficiently and easily.

As has been described previously, the film 30 is attached to the mold 20 so that it does not have any deformation. The cavity surface 24a of the upper mold 21 is flat. The film 30 has a uniform quality and even elasticity on the whole surface thereof. Hence, the bumps 12 equally fall in the film 30.

Hence, the ends of the bumps 12 equally protrude from the resin layer 13, and the semiconductor devices 10 have a uniform quality and uniform contacts with the connection electrodes 15.

In the above description, the ends of the bumps 12 are completely exposed from the resin layer 13 after the film 30 is detached from the resin layer 13 by the protruding electrode exposing step. Alternatively, the ends of the bumps 12 may slightly be covered by a resin film (the sealing resin 35) after the film 30 is detached. With the above structure, the upper ends of the bumps 12 that are liable to take scratches are protected by the resin

mechanism 40.

The excess resin removing mechanism 40 is generally made up of an opening part 41, a pot part 42, and a pressure control rod 43. The opening part 41 is an opening formed in a part of the slant portion 27 formed in the second lower mold half body 24A, and is connected to the pot part 42.

The pot part 42 has a cylinder structure. The pressure control rod 43 having a piston structure is slidably provided in the pot part 42. The pressure control rod 43 is connected to a driving mechanism which is not shown, and can be elevated with respect to the second lower mold half body 24A in the direction Z1 and Z2.

Next, a description will be given of the semiconductor device fabrication method using the mold 20A equipped with the excess resin removing mechanism 40 according to the second embodiment of the present invention. The second embodiment is characterized in the resin sealing step, and only a description thereof will be given below.

The resin sealing step commences executing a substrate loading step, in which the substrate 16 is loaded onto the mold 20A as shown in Fig. 10(A).

As shown in this figure, the second lower mold half body 24A is spaced apart from the first lower mold half body 23 along the direction Z2 immediately after the resin sealing step is initiated. Further, the pressure control rod 43 of the excessive resin removing mechanism 40 is placed in a position in the direction Z2.

After the substrate 16 is loaded onto the lower mold 22A, the film 30 is disposed to the part 24a of the upper mold 21, and the sealing resin 35 is placed on the substrate 16 or the bumps 12 provided thereon.

After the above substrate loading step is

completed, a resin layer forming step is executed. The upper mold 21 is moved in the direction Z1. Then, as shown in Fig. 10(B), the upper mold 21 and the second lower mold half body 24A come into contact with each other, so that the film 30 is brought in the clamped state.

At this time, the cavity 28 is defined in the mold 20A by the cavity surfaces 24a, 25 and 26. The opening part 41 of the excess resin removing mechanism 40 is opened to the cavity 28.

After the upper mold 21 comes into contact with the second lower mold half body 24A, the upper mold 21 and the second lower mold half body 24A maintains the film 30 in the clamped state while moving in the direction Z1 as a whole. Hence, the resin 35 is compressed and molded in the cavity 28.

In order to prevent the bumps 12 from being damaged and appropriately fill the whole cavity 28 with the resin 35, it is necessary to select an appropriate moving speed of the upper mold 21 and the second lower mold half body 24A in the direction Z1, as has been described previously. The appropriate value selecting of the speed of the upper mold 21 and the second lower mold half body 24A in the direction Z1 is equivalent to the appropriate value selecting of the pressure applied to the resin 35 in the cavity 28.

According to the second embodiment of the present invention, the mold 20A is equipped with the excess resin removing mechanism 40. Hence, it is possible to control not only the moving speed of the upper mold 21 and the second lower mold half body 24A in the direction Z1 but also the compression pressure applied to the resin 35 using the pressure control rod 43. When the pressure control rod 43 reduces a pressure exerted in the direction Z2, the sealing resin 35 receives a reduced pressure in the cavity 28. When the pressure control rod 43 increases a pressure

body 24A with respect to the first lower mold half body 23 in the direction Z1, the resin layer 13 can be detached from the slant portion 27.

In the second embodiment of the present invention, there is a possibility that the excess resin removing mechanism 40 may form a flash in the position in which the opening part 41 is located. Such a flash can be removed by moving the second lower mold half body 24A in the direction Z1.

After the resin layer 13 is separated from the slant portion 27, the second lower mold half body 24A is moved in the direction Z2, so that the upper surface of the half body 24A comes into contact with the film 30 and the slant portion 27 comes into contact with the resin layer 13 again. Hence, the substrate 16 is urged in the direction along which it is away from the mold 20A. Hence, as shown in the right side with respect to the center line in Fig. 10(D), the substrate 16 to which the resin layer 13 is provided is separated from the mold 20A.

In the fabrication method of the second embodiment of the present invention, the pressure in the cavity 28 can be regulated at the predetermined level. Hence, it is possible to prevent air from remaining in the resin 35 and prevent babbles (voids) from being formed in the resin layer 13. If babbles occur in the resin layer 13, these bobbles are expanded in a thermal process and a damage such as a crack may occur in the resin layer 13.

The excess resin removing mechanism 40 can prevent babbles from being formed in the resin layer 13 and prevent the resin layer from being damaged in the thermal process. Hence, the reliability of the semiconductor device 10 can be improved.

A description will now be given of a semiconductor device fabrication method according to third and fourth embodiments of the present invention.

Fig. 11 shows the semiconductor device fabrication method according to the third embodiment of the present invention, and Fig. 12 shows the semiconductor device fabrication method according to the fourth embodiment of the present invention. In Fig. 11, parts that have the same structures as those of the first embodiment of the present invention which has been described with reference to Figs. 1 through 9 are given the same reference numbers. In Fig. 12, parts that have the same structures as those of the first embodiment of the present invention which has been described with reference to Fig. 10 are given the same reference numbers.

The fabrication methods according to the third and fourth embodiments of the present invention are characterized in that the resin layer 13 is formed without using the film 30. As shown in Figs. 11(A) and 12(A), the film 30 is not arranged to the portion 24a of the upper mold 21 in the substrate loading. This differs from the first and second embodiments of the present invention.

Hence, in the resin layer forming step subsequent to the substrate loading step, as shown in Figs. 11(B), 11(C), 12(B) and 12(C), the upper mold 21 directly pushes the sealing resin 35, which is compression-molded. Since the cavity surface 24a of the upper mold 21 is flat, the resin layer 13 is molded under the good condition. The removing process is the same as that of the first or second embodiment of the present invention, and a description thereof will be omitted.

The resin layer 13 can be formed without using the resin layer 13. It should be noted that the bumps 12 completely fall in the resin layer 13 when the resin layer 13 is formed because the film 30 is not employed.

Hence, it is necessary to expose only the

the substrate loading step commences moving the upper mold 21 and the second lower mold half body 24 in the direction Z1 so that the step of sealing the bumps 12 by the sealing resin 35 is initiated. At this time, the mold 20 is heated up to a temperature at which the sealing resin 35 can be fused. The above-mentioned thermosetting adhesive is formed of a material which is thermohardened at a comparatively low temperature. Hence, the reinforcement plate 50 is unified to the substrate 16 with a relatively short time after the initiation of the resin layer forming step. The reinforcement plate 50 may adhere to the substrate 16 beforehand.

As shown in Figs. 13(B) and 13(C), the resin layer 13 is formed by the compression molding method even in the fifth embodiment of the present invention. In the above method, the resin in the fused state is pressed by the upper mold 21, and the substrate receives a large pressure.

The formation of the resin layer 13 requires fusing of the sealing resin 35. Hence, the mold 20 is equipped with a heater. Heat generated by the heater is applied to the substrate 16 loaded onto the mold 20. Hence, the substrate 16 may be deformed due to the pressure in the compression molding and the heat of the heater. According to the fifth embodiment of the present invention, the reinforcement plate 50 is loaded before the substrate 16 is loaded onto the mold 20 in the substrate loading step, and is bonded to the substrate 16. Hence, the substrate 16 is reinforced by the reinforcement plate 50 in the resin layer forming step. Hence, even if the substrate 16 receives a pressure in the compression molding and heat of the heater, the substrate 16 can be prevented from being deformed and the yield can be improved.

Fig. 14 shows the substrate 16 which has been removed from the mold 20 after the resin layer 13

is completely formed. As shown in that figure, the reinforcement plate 50 is still attached to the substrate 16 even after the substrate 16 is removed from the mold 20. In the separating step (see Fig. 8) carried out by the resin layer forming step, the reinforcement plate 50 is cut by the dicer 29.

Thus, the separated semiconductor chips have the respective pieces of the reinforcement plate 50. As described before, the reinforcement plate 50 is made of a substance having a good heat radiation performance. Hence, the pieces of the reinforcement plate 50 of the semiconductor devices function as heat radiating plates. Thus, each semiconductor device has an improved heat radiating performance.

Figs. 15 through 17 show variations of the above-mentioned embodiments of the present invention. In these figures, parts that have the same structures as those of the aforementioned embodiments of the present invention are given the same reference numbers.

In the above-mentioned embodiments of the present invention, the sealing resin 35 is placed on the substrate 16 on the mold 20 or 20A. In the variations shown in Figs. 15 through 17, sealing resin is supplied in different manners.

The variation shown in Fig. 15 is characterized by using a sheet resin 51. The sheet resin 51 makes it possible to definitely form the resin layer 13 on the whole substrate 16.

When the sealing resin 35 is disposed on the center of the substrate 16, it takes a long resin formation time for melted resin to flow to the ends of the substrate 16 from the center thereof. In contrast, the sheet resin 51 is arranged so as to cover the upper portion of the substrate 16, the melted resin directly seals the bumps 12 located below the sheet resin 51 rather than flowing to the ends of

not provided) are loaded onto the mold 20 (that is, the substrate loading step is executed). Hence, the state shown in Fig. 18(A) is obtained. Then, the above process is repeatedly carried out.

According to the method of this embodiment, the sealing resins 35A are arranged so as to be spaced apart from each other at given intervals which do not affect the resin sealing step. The film 30 is transported when the resin sealing step is completed. The sealing resin 35A for the next resin sealing step is automatically loaded onto the mold 20. Hence, the resin sealing step is repeatedly carried out, and the efficiency in fabrication of the semiconductor devices can be improved.

Figs. 19 through 21 are diagrams for explaining a method for fabricating a semiconductor device according to a seventh embodiment of the present invention. In Figs. 19 through 21, parts that have the same structures as those of the first embodiment of the present invention which has been described with reference to Figs. 1 through 9 are given the same reference numbers, and a description thereof will be omitted.

In the aforementioned fabrication method according to the first embodiment of the present invention, the film 30 is formed of a flexible substance which is elastically deformable. In the resin sealing step, the ends of the bumps 12 are make to fall in the film 30. Hence, merely by detaching the film 30 from the resin layer 13 in the protruding electrode exposing step, the ends of the bumps 12 are exposed.

It may be slightly difficult to arrange the film 30 having an elasticity which allows only the ends of the bumps 1 to fall in the film 30. In the case where the film 30 is used as a carrier for transportation as shown in Fig. 18, the film 30 made

bumps 12 can precisely be exposed with ease. If etching, mechanical polishing or blasting is used, the ends of the bumps 12 can be exposed at a comparatively low cost.

A description will now be given, with reference to Figs. 22 through 25, of a mold 20C for the semiconductor device fabrication method according to the third embodiment of the present invention (hereinafter simply referred to as mold 20C). In Figs. 22 through 25, parts that have the same structures as those of the mold 20 shown in Fig. 1 are given the same reference numbers, and a description thereof will be omitted.

The mold 20C is characterized by providing a fixing/detaching mechanism 70 for fixing the substrate 16 to the first lower mold half body 23C or detaching it therefrom to the position in which the first lower mold half body 23C is placed. The fixing/detaching mechanism 70 is generally made up of a porous member 71, an intake/exhaust device 73 and a pipe 74.

The porous member 71 is formed of a porous ceramic, a porous metal or a porous resin, through which a gas (such as air) can pass.

The pipe 73 is arranged below the porous member 71, and is connected to the intake/exhaust device 72. The intake/exhaust device 72 may be a compressor or a negative pressure generator, and has a compressed gas feed mode in which compressed air is fed to the pipe 73, and a suction mode in which a suction process is carried out for the pipe 73. The intake/exhaust device 72 can switch between the above two modes.

When the intake/exhaust device 72 operates in the compressed gas feed mode, the compressed air is supplied to the porous member 71 via the pipe 73, and is then injected to the outside of the device 72. At this time, if the substrate 16 is placed on the first

center line of Fig. 24 shows a state in which the second lower mold half body 24E moves up, and the substrate 16 to which the resin layer 13 is attached is detached from the mold 20E.

Fig. 25 shows a mold 20F for the semiconductor device fabrication method according to the sixth embodiment of the present invention (hereinafter simply referred to as mold 20F).

The mold 20F used in the present embodiment is characterized by providing non-adhesive process films 75 in an interface between contact surfaces of an upper mold 21F and a lower mold 22F (a first lower mold half body 23F and a second lower mold half body 24F), the resin layer 13 being placed on the above contact surfaces. The non-adhesive process films 75 are made of a substance which does not adhere to the resin layer 13. Hence, the substrate 16 to which the resin layer 13 is formed can be detached from the mold 20F with ease.

Figs. 76 and 77 show a variation of the mold used in the sixth embodiment of the present invention. Fig. 76 shows an arrangement in which the area of the substrate 16 is narrower than the upper area of the first lower mold half body 23, and a film 30D is placed on the upper surface of the sealing resin 35. Hence, it is possible to reduce the contact interface between the sealing resin 35 and the first lower mold half body 23 and facilitate the detachability.

When a suction process as described with reference to Fig. 22 is employed in the present embodiment, fine holes (vacuum holes) may be provided in necessary positions of the film 30D.

Fig. 77 shows an arrangement in which the area of the upper surface of the first lower mold half body 23 is approximately equal to the area of the substrate 16. In each of the aforementioned embodiments, the area of the substrate 16 is narrower

than the area of the upper surface of the first lower mold half body 23. Hence, the resin layer 13 is provided on sides of the substrate 16 (side surface portions) by the resin sealing process.

By making the area of the upper surface of the first lower mold half body 23 and the area of the substrate 16 equal to each other, it is possible to form the resin layer 13 on the upper surface of the substrate 16 only. It is possible to selectively provide the resin layer 13 on the upper surface of the substrate 16 only or not only on the upper surface but also the side surfaces by taking into consideration how the substrate 16 is used.

In the structure shown in Fig. 77, the film 30 is used for the upper mold 21 and the non-adhesive process film 75 (Fig. 25) is used for the lower mold 22 in order to facilitate the detachability.

A description will now be given of semiconductor devices according to second and third embodiments of the present invention.

Fig. 26 shows a semiconductor device 10A according to the second embodiment of the present invention, and Fig. 27 shows a semiconductor device 10B according to the third embodiment of the present invention. In Figs. 26 and 27, parts that have the same structures as those of the semiconductor device 10 shown in Fig. 9 according to the first embodiment of the present invention are given the same reference numbers.

The semiconductor device 10A according to the second embodiment of the present invention has a module structure in which a plurality of semiconductor elements 11 are mounted on a stage member 80. The resin layer 13 seals the bumps 12 except for the ends thereof, and seals the side portions of the semiconductor elements 11. Further, the stage member 80 is formed of a substance having good heat radiating

A description will now be given of an eight embodiment of the present invention. Fig. 28 is a diagram which shows a method for fabricating a semiconductor device according to the eighth embodiment of the present invention and more particularly illustrates the substrate 16 after the resin sealing step is completed. Fig. 28(A) shows the whole substrate 16, and Fig. 28(B) is an enlarged view of a portion of the substrate 16. In Fig. 28, parts that have the same structures as those of the first embodiment of the present invention which has been described with reference to Figs. 1 through 9 are given the same reference numbers, and a description thereof will be omitted.

The aforementioned method for fabricating the semiconductor device according to the first embodiment of the present invention employs the resin layer 13 formed by a single kind of resin layer 35. It will be noted that the resin layer 13 is required to have various functions. For example, it is desirable to form the resin layer 13 of hard resin in terms of protection of the substrate 16 and to form the resin layer 13 of soft resin in order to relax stress applied to the bumps 12 when mounting the device. In practice, it may be very difficult to meet both the requirements by means of a single kind of resin.

The eight embodiment of the present invention is characterized in that a plurality of kinds of resin having different natures are used as the sealing resin used in the resin sealing step. In the present embodiment, two kinds of resin are used to form resin layers 13A and 13B. In the example shown in Fig. 28, the resin layers 13A and 13B are stacked.

In order to form the resin layers 13A and 13B, the resin molding step commences filling the mold with sealing resin for forming the resin layer 13A.

Then, the resin layer 13A is formed on the substrate 16. Next, the resin molding step fills the mold with sealing resin for forming the resin layer 13B. Hence, the resin layer 13B is formed on the resin layer 13A. Alternatively, a sealing resin is formed beforehand which has a stacked structure having the resin layers 13A and 13B. Then, the above sealing resin is formed on the substrate 16 so that the resin layers 13A and 13B are provided by performing the resin sealing step only one time.

For example, the resin layer 13B facing the outside of the device is made of hard resin, and the resin layer 13A located inside thereof is made of soft resin. In this arrangement, the substrate 16 can definitely be protected by the resin layer 13B formed of hard resin, while stress applied to the bumps 12 at the time of mounting the device can be absorbed by the resin layer 13A formed of soft resin. Hence, the semiconductor device fabricated by the present embodiment method has improved reliability.

A description will now be given of a ninth embodiment of the present invention.

Fig. 29 is a diagram showing a method for fabricating a semiconductor device according to the ninth embodiment of the present invention. In Fig. 29, parts that have the same structures as those of the first embodiment of the present invention are given the same reference numbers, and a description thereof will be omitted.

The ninth embodiment of the present invention is characterized, as in the case of the eighth embodiment thereof, by using a plurality kinds of resin having different performances are used (two kinds of resin are used in the ninth embodiment). The eighth embodiment of the present invention has the stacked structure made up of the resin layers 13A and 13B. In the ninth embodiment of the present

tenth embodiment of the present invention, and Fig. 31 is a diagram showing a method for fabricating a semiconductor device according to the eleventh embodiment of the present invention. In Figs. 30 and 31, parts that have the same structures as those of the first embodiment described with reference to Figs. 1 through 9 and the ninth embodiment of the present invention described with reference to 29 are given the same reference numbers.

The fabrication method according to the tenth embodiment shown in Fig. 30 is characterized by arranging the sealing resin 35 to the reinforcement plate 50 in the resin sealing step as in the case of the aforementioned ninth embodiment of the present invention. The fabrication method according to the eleventh embodiment shown in Fig. 31 is characterized by providing a reinforcement plate 50A integrally with a frame part 54 and arranging the sealing resin 35 to the reinforcement plate 50A beforehand.

By arranging the sealing resin 35 to the reinforcement plates 50 and 50A beforehand in the resin sealing step, the reinforcement plates 50 and 50A can be used as a part of the mold 20G. More particularly, the reinforcement plates 50 and 50A can be used as a part of the first lower mold half body 23.

Hence, it is possible to reduce the area of the sealing resin 35 which directly contacts the first lower mold half body 23 (mold 20G) and to omit the step of removing unwanted resin attached to the mold employed in the prior art. Hence, the work of the resin sealing step can be simplified.

Particularly, the eleventh embodiment of the present invention provides the reinforcement plate 50A with the frame part 54. Hence, the portion of the reinforcement plate 50A which faces the substrate 16 defines a recess portion 55, which can be used as a cavity. In the arrangement shown in Fig. 30 in which the reinforcement plate 50 of a flat-plate shape is used, the sealing resin 35 touches the second lower mold half body 24. Hence, unwanted resin located in the above touching portion cannot be removed.

In contrast, the eleventh embodiment of the present invention shown in Fig. 31 can realize an arrangement in which the sealing resin 35 does not contact the mold 30G at all, so that unwanted resin attached to the mold 20G can easily be removed.

In the above-mentioned tenth and eleventh embodiments of the present invention, when the reinforcement plates 50 and 50A are formed of a material having a good heat radiating performance, the semiconductor devices 10D and 10E will have an improved heat radiating performance. Fig. 30(B) shows the semiconductor device 10D fabricated by the fabrication method according to the tenth embodiment, and Fig. 31(B) shows the semiconductor device 10E fabricated by the fabrication method according to the eleventh embodiment of the present invention.

A description will now be given of a twelfth embodiment of the present invention.

Figs. 32 and 33 are diagrams showing a method for fabricating a semiconductor device according to the twelfth embodiment of the present invention. In Figs. 32 and 33, parts that have the same structures as those of the first embodiment described with reference to Figs. 1 through 9 are given the same reference numbers, and a description thereof will be omitted.

The fabrication method of the present

resin, the substrate 16 can definitely be protected from external force. When the second resin layer 17 is formed of resin having a good heat radiating performance, the semiconductor device 10E has an improved heat radiating performance.

A description will be given of a thirteenth embodiment of the present invention.

Fig. 34 is a diagram showing a method for fabricating a semiconductor device according to a thirteenth embodiment of the present invention. In Fig. 34, parts that are the same as those of the first embodiment described with reference to Figs. 1 through 9 and the twelfth embodiment described with reference to Figs. 32 and 33 are given the same reference numbers, and a description thereof will be omitted.

Even in the present embodiment fabrication method, the first resin layer 13 is formed on the front surface of the substrate 16 and the second resin layer 17 is formed on the back surface thereof. In the fabrication method of the twelfth embodiment described with reference to Figs. 32 and 33, the first resin layer 13 is formed by the process shown in Fig. 32(A) through 32(C). Thereafter, the substrate 16 to which the first resin layer 13 is formed is taken out of the mold 20 and is turned upside down. Then, the process shown in Figs. 33(D) through 33(F) is carried out so that the second resin layer 17 is formed. Hence, the twelfth embodiment of the present invention is required to perform the compression molding step twice and does not have a good production efficiency.

With the above in mind, the fabrication method according to the thirteenth embodiment of the present invention is characterized by simultaneously forming the first and second resin layers 13 and 17 by carrying out the compress molding step only one time. When the substrate 16 is loaded onto the mold 20 in the resin sealing step, as shown in Fig. 34(A), the

shown by an enlarged illustration of Fig. 35(D), the straight bumps 18 are embedded in the resin layer 13 except for the ends thereof.

In the seventh embodiment described with reference to Figs. 19 through 21, the bumps 12 has a spherical shape, and thus only small areas of the bumps 12 are exposed from the resin layer 13 which totally seals the bumps 12. Hence, it is required to expose the ends of the bumps 12 from the resin layer 13, as shown in Fig. 21.

In contrast, the fourteenth embodiment of the present invention employs the straight bumps 18 of the circular cylinder shape, the ends of the bumps 18 exposed from the resin layer 13 has a comparatively wide area. Hence, as shown in Fig. 35(D), a sufficient electrical contact can be made by merely removing the film 30A from the resin layer 13. Hence, the use of the straight bumps 18 can omit the step of exposing the bumps 12 from the resin layer 13 which is required when the spherical bumps 12 are employed. Thus, the step of fabricating the semiconductor device can be simplified.

If it is required to provide further improved electrical contact performance, the step of exposing the ends of the straight bumps 18 from the resin layer 13. In the following description, the term "bumps 12" includes the bumps 12 having the spherical shape and the straight bumps 18. Further, if the bumps 12 having the spherical shape are specifically described, a term "spherical bumps 12" is used. Similarly, if the straight bumps 18 are specifically described, a term "straight bumps 18" is used.

A description will be given of a fifteenth embodiment of the present invention.

Fig. 36 is a diagram showing a method of fabricating a semiconductor device according to the

fifteenth embodiment of the present invention. In Fig. 36, parts that have the same structures as those of the first embodiment described with reference to Figs. 1 through 9 and the fourteenth embodiment described with reference to Fig. 35 are given the same reference numbers, and a description thereof will be omitted.

The fabrication method according to the fifteenth embodiment is characterized by forming, after at least the ends of the bumps 12 (the straight bumps 18 are used in the present embodiment) are exposed from the resin layer 13 by the protruding electrode exposing step, other bumps 90 (hereinafter referred to as external connection bumps) on the ends of the bumps 12.

The external connection bumps 90 are formed by an external connection protruding electrode forming step, which may be a bump formation technique which is generally used in practice. Examples of such a technique are a transferring method, a plating method and a dimple plate method. After the protruding electrode exposing step is executed, the external connection protruding electrode forming step is carried out so that the external connection bumps 90 are formed on the ends of the straight bumps 18.

According to the present embodiment, the protruding electrode exposing step is carried out and then the external connection protruding electrode forming step is carried out so that the external connection bumps 90 are formed on the ends of the straight bumps 18 and the electrical connections between the semiconductor device and a mounting board can be made more definitely.

More particularly, the bumps 12 are formed on the electrodes formed on the substrate 16 (semiconductor element), and are required to have a small size. Hence, when the small-size bumps 12 are

In Fig. 38, an illustration of the mold is omitted.

Fig. 38(B) shows a state in which the substrate 16, the sealing resin 35 and the film 30B are loaded onto the mold. In this state, the projections 19 formed on the film 30B are positioned so as to face the bumps 12 formed on the substrate 16. The film 30B is formed of a hard resin substance, and the projections 19 are formed of a comparatively soft resin substance. That is, the present embodiment, the film 30B and the projections 19 are made of different substances (however, the films 30B and the projections 19 may be integrally formed of an identical substance).

Fig. 38(C) shows a state in which the sealing resin 35 is subjected to a compression molding process. In the compression molding process, the projections 19 formed on the film 30B are pressed by the bumps 12. Hence, the sealing resin 35 do not adhere to the bumps 12, in areas in which the projections 19 are pressed by the bumps 12. IN addition, the projections 19 are formed of soft resin, and the contact areas between the bumps 12 and the projections 19 can be increased because the projections 19 are elastically deformable.

Fig. 38(D) shows a protruding electrode exposing step in which the film 30B is removed from the substrate 16. As has been described previously, the sealing resin 35 do not adhere to the bumps 12 in the areas in which the bumps 12 are pressed by the projections 19. In the state in which the film 30B has been removed, the above areas are exposed from the resin layer 13. In addition, the areas in which the bumps 12 are exposed from the resin layer 13 are wider than corresponding those obtained by the method of the first embodiment of the present invention.

Hence, according to the seventeenth embodiment of the present invention, it is possible to

definitely expose the bumps 12 from the resin layer 13 without a large scale facility. Further, the areas of the bumps 12 exposed from the resin layer 13 are comparatively wide. Hence, as shown in Fig. 38(E), even when the external connection bumps 90 are provided to the ends of the bumps 12, the bumps 12 and the external connection bumps 90 can definitely be bonded together.

A description will be given of an eighteenth embodiment of the present invention.

Figs. 39 and 40 are diagrams showing a method for fabricating a semiconductor device according to the eighteenth embodiment of the present invention. In Figs. 39 and 40, parts that have the same structures as those of the first embodiment described with reference to Figs. 1 through 9 are given the same reference numbers and a description thereof will be omitted.

The present embodiment is characterized by a method for forming a bump 12A on the substrate 16 and a structure thereof. The bump 12A is formed on a connection electrode 98 provided on the surface of the substrate 16. The step of forming the bump 12A commences forming a core portion 99 (indicated by a pear-skin illustration) on the upper portion of the connection electrode 98. The core portion 99 is formed of resin having elasticity (for example, polyimide).

The core portion 99 can be formed on the connection electrode 98 by the following method. First, resin (photosensitive polyimide) for forming the core portion 99 is spin-coated on the entire surface of the substrate 16 to have a given thickness. Subsequently, the portion of the resin 98 other than the connection electrode 98 is removed by photolithography.

Then, an electrically conductive film 100 is

formed so as to cover the entire surface of the core portion 99. The electrically conductive film 100 is formed by a thin-film forming technique such as a plating method or sputtering method. The side portions of the film 100 are connected to the connection electrode 98. The electrically conductive film 100 is formed of a metal which has an elasticity and a low electrical resistance. By the above method, the bump 12A is formed. In Fig. 39, a reference number 102 indicates an insulating film.

It can be seen from the above description that the bump 12A includes the core portion 99 and the electrically conductive film 100 formed on the surface of the core portion 99. As described above, the core portion 99 has an elasticity and the electrically conductive film 100 is also formed by a substance having en elasticity. Hence, even if external force is exerted on the bump 12A at the time of mounting, resultant stress can be absorbed due to elastic deformations of the core portion 99 and the electrically conductive film 100. Hence, it is possible to prevent stress from being applied to the substrate 16, which can thus be suppressed from being damaged.

Now, a description will be given of the height of the bump 12A with respect to the resin layer 13. Fig. 39(A) shows an arrangement in which the ends of the bump 12A protrudes from the resin layer 13. The bump 12A has a comparatively wide exposed area. Hence, when the external connection bump 90 is provided, the bump 21A and the bump 90 can definitely be bonded together through a wide interface area.

Fig. 39(B) shows an arrangement in which the end of the bump 12A is flush with the surface of the resin layer 13. This arrangement provides a semiconductor device of an LCC (Leadless Chip Carrier) structure, and contributes to increasing the mounting

density.

Fig. 39(C) shows an arrangement in which the end of the bump 12A is located at a lower level than that of the surface of the resin layer 13. Hence, a recess portion 101 is formed in the resin layer 13 through which the bump 12A is exposed. If the external connection bump 90 is applied to the present arrangement, the recess portion 101 functions to position the external connection bump 90. Hence, as compared with the arrangement shown in Fig. 39(A), the bump 12A and the external connection bump 90 can be positioned easily.

In the present eighteenth embodiment, as shown in Fig. 40, electrode pads 97 provided on the substrate 16 (semiconductor element) are spaced apart from connection electrodes 98 in which the bumps 12A are formed. The electrode pads 97 and the connection electrodes 98 are connected together through lead lines 96.

In the arrangement shown in Fig. 39 in which the external connection bump 90 is provided to the end of the bump 12A, the bump 90 is made greater than the bump 12A in order to improve the mounting performance. Hence, if the adjacent bumps 12 are arranged at a small pitch, the adjacent external connection bumps 90 may contact each other.

With the above in mind, in the arrangement shown in Fig. 90, the electrode pads 97 and the connection electrodes 98 are connected together by means of the lead lines 96, so that the connection electrodes 98 in which the bumps 12A are formed are arranged at an increased pitch. Hence, it is possible to avoid occurrence of an interference between the adjacent external connection bumps 90.

A description will be given of a nineteenth embodiment of the present invention.

Fig. 41 is a diagram showing a method for

producing a semiconductor device according to the nineteenth embodiment of the present invention. In Fig. 41, parts that have the same structures as those of the first embodiment described with reference to Figs. 1 through 9 are given the same reference numbers, and a description thereof will be omitted.

In the present fabrication method, as shown in Fig. 41(A), a cut position groove 105 having a relatively wide width is formed, before the resin sealing step, in a position (indicated by a broken line X; the position is hereinafter referred to as cut position) in which the substrate 16 is cut by a separating step carried out. The width of the cut position groove 105 is at least greater than the width of a dicer 29, which will be described later.

In the resin sealing step of forming the resin layer 13 subsequent to the step of forming the groove 105, the cut position groove 105 is filled with the sealing resin 35, so that a cut position resin layer 106 is formed. In the separating step carried out after the resin sealing step, as shown in Fig. 41(B), the substrate 16 is cut, by the dicer 29, in the cut position X within the cut position groove 105 full of the cut position resin layer 106. Hence, the substrate 16 is cut as shown in Fig. 41(C).

According to the above mentioned fabrication method, it is possible to prevent occurrence of a crack in the substrate 16 and the resin layer 13 in the separating step. The reason for the above will be described below.

An arrangement will now be assumed in which the cut position groove 105 is not formed. The separating step cuts the substrate 16 having the surface on which the resin layer 13 that is a relatively thin film is provided. The cutting process using the dicer 29, a large magnitude of stress is applied to the substrate 16. Hence, the thin resin

layer 13 may be flaked off from the substrate 16 or crack may occur in the resin layer 13 and the substrate 16.

In contrast, according to the nineteenth embodiment of the present invention, the cut position groove 105 which is relatively wide is formed in the cut position X. Hence, the separating step is carried out within the cut position groove 105 in which the cut position resin layer 106 is formed. The cut position resin layer 106 is thicker than the resin layer 13 formed on the other portion, and a greater mechanical strength. Further, the cut position resin layer 106 is more flexible than the substrate 16, and functions to absorb the stress.

Hence, the stress caused in the cutting process is absorbed and weakened by the cut position resin layer 106, and is then applied to the substrate 16. Hence, it is possible to prevent occurrence of a crack in the resin layer 13 and the substrate 16 and improve the yield.

As shown in Fig. 41(C), exposed portions of the cut position resin layer 106 are provided on the side surfaces of the substrate 16 after the separating step is completed. Hence, the side portions of the substrate 16 are protected by the cut position resin layer 106, so that the substrate 16 can be suppressed from being affected by the external environments.

Further, a handling apparatus used to transport the semiconductor device can be designed to grip the exposed portions of the cut position resin layer 106. Hence, it is possible to prevent the substrate 16 from being damaged by the handling apparatus.

A description will now be given of a twentieth embodiment of the present invention.

Fig. 42 is a diagram showing a method for fabricating a semiconductor device according to the

cutting portion 16a is cut is transferred towards the sides of the substrate 16. However, the stress relaxing grooves 110a and 11b full of the stress relaxing layers 111a and 111b are formed on the sides of the substrate cutting portions 16a. Hence, the above stress can be absorbed by the stress relaxing grooves 110a and 110b.

Hence, the stress generated in the substrate cutting portions 16a do not affect portions (in which electronic circuits are formed) located beyond the stress relaxing grooves 110a and 110b. Thus, it is possible to prevent a crack from being generated in the areas in which the bumps 12 and electronic circuits are formed. Fig. 42(C) shows a state in which the separating step is completed.

A description will be given of a twenty first embodiment of the present invention.

Fig. 43 is a diagram of a method for fabricating a semiconductor device according to the twenty first embodiment. In Fig. 43, parts that have the same structures as those of the first embodiment described with reference to Figs. 1 through 9 and the nineteenth embodiment described with reference to Fig. 41 are given the same reference numbers, and a description thereof will be omitted.

In the fabrication method of the present embodiment, a first separating step is executed before the resin sealing step is executed. Thus, the substrate 16 is separated into semiconductor elements 112. Each of the semiconductor elements 112 is equipped with bumps 12 and an electronic circuit (not shown).

After the first separating step is completed, the resin sealing step is carried out. In this step, as shown in Fig. 43(A), the semiconductor elements 112 are arranged on a film member 113 serving as a base member. At this time, an adhesive is used

given the same reference numbers and a description thereof will be omitted.

The fabrication method of the present embodiment is characterized by forming, as shown in Fig. 46, positioning grooves 120 on the resin layer after the resin sealing step is executed but before the separating step is executed.

The positioning grooves 120 formed on the resin layer 13 can be used as a reference for positioning a semiconductor device 10F to a tester. By forming the positioning grooves 120 before the separating step is executed, the positioning grooves 120 can be totally and efficiently formed with respect to a plurality of semiconductor devices 10F.

The positioning grooves 120 can be formed by, for example, performing half scribing to the resin layer 13 by using the dicer 29, as shown in Fig. 45. Hence, the positioning grooves 120 can be efficiently and precisely formed by the generally used scribing technique.

A description will be given of a twenty fourth embodiment of the present invention.

Fig. 47 is a diagram showing a method for fabricating a semiconductor device according to the twenty fourth embodiment. In Fig. 47, parts that have the same structures as those of the first embodiment are given the same reference numbers and a description thereof will be omitted.

The present embodiment is characterized by forming, as shown in Fig. 47, positioning grooves 121 on the back surface of the substrate 16 before the resin sealing step is completed but before the separating step is performed. Fig. 47(B) is an enlarged view of a part of the illustration of Fig. 47(A).

The positioning grooves 121 can be used as a reference for positioning the semiconductor device as

in the case of the twenty third embodiment. Particularly, the positioning of the semiconductor device at the time of mounting is carried out so that the bumps 12 face the mounting board. Hence, the positioning grooves 120 formed on the resin layer 13 cannot be visually recognized from the upper side.

In contrast, the positioning grooves 121 formed on the back surface of the substrate 16 can be visually recognized even at the time of mounting. Hence, the mounting process can be carried out precisely. The positioning grooves 121 can be formed by performing half scribing on the back surface of the substrate 16 by the dicer 29 as in the case of the twenty third embodiment.

A description will be given of twenty fifth and twenty sixth embodiments of the present invention.

Fig. 48 is a diagram showing a method for fabricating a semiconductor device according to the twenty fifth embodiment of the present invention, and Fig. 49 is a diagram showing a method for fabricating a semiconductor device according to the twenty sixth embodiment of the present invention. In Figs. 48 and 49, parts that have the same structures as those of the first embodiment described with reference to Figs. 1 through 9 are given the same reference numbers, and a description thereof will be omitted.

The fabrication method of the twenty fifth embodiment is characterized by forming positioning grooves 121 as in the case of the twenty third and twenty fourth embodiments. Fig. 48(C) shows one positioning groove 1 22 formed on the resin layer 13.

As shown in Fig. 48(A), the positioning grooves 122 are formed by using a film 30C having projections 31 located in positions in which the projections 31 do not interfere with the bumps 12. Fig. 48(B) shows a state in which the film 30C having the projections 31 faces the substrate 16 in the resin

sealing step. As shown, the projections 31 is located so as not to face the bumps 12. Hence, the positioning groove 122 is formed on the resin layer 13 due to the projections 31 when the resin sealing step is completed.

The fabrication method of the twenty sixth embodiment is characterized by forming a positioning protruding 123 in the resin layer 13. Fig. 49(C) shows the positioning protruding 123 formed in the resin layer 13.

The positioning protruding 123 are formed by using the film 30C having recesses 32 located in the positions in which the recess positions 32 do not interfere with the bumps 12. Fig. 49(B) shows a state in which the film 30C having the recess 32 faces the substrate 16. As shown, the recess 32 is located so as not to face the bumps 12. Hence, the positioning protruding 123 is formed on the resin layer 13 due to the recess 32 when the resin sealing step is completed.

The above-mentioned twenty fifth and twenty sixth embodiments respectively use the films 30C having the projections 31 and the recesses 32 located in the positions having no positional interferences with the bumps 12, so that the positioning grooves 122 and the positioning protruding 123 serving as the references for positioning can be formed on the resin layer 13. Hence, when the semiconductor device is subjected to a test process or a mounting process, the semiconductor device can be positioned by referring to the positioning grooves 122 or the positioning protruding 123. Hence, the positioning work of the semiconductor device can be simplified.

A description will be given of a twenty seventh embodiment of the present invention.

Fig. 50 is a diagram showing a method for fabricating a semiconductor device according to the

twenty seventh embodiment. In Fig. 50, parts that have the same structures as those of the first embodiment described with reference to Figs. 1 through 9 are given the same reference numbers, and a description thereof will be omitted.

The fabrication method of the present embodiment is characterized by selecting some bumps 12 among the bumps 12 as references for positioning (hereinafter such bumps are referred to as positioning bumps 12B) and by processing, after the resin sealing step is completed, the resin layer 13 in the positions in which the positioning bumps 12B are formed. Hence, the general bumps 12 can be discriminated over the positioning bumps 12B. The structure itself of the positioning bumps 12B is the same as that of the general bumps 12.

Fig. 50(A) shows the substrate 16 observed after the resin sealing step and the protruding electrode exposing step are completed. In this state, the resin layer 13 has a uniform film thickness on the substrate 16. Hence, the positioning bumps 12B cannot be discriminated from the general bumps 12.

With the above in mind. as shown in Fig. 50(B), a step is performed which reduces the thickness of the resin layer 13 in the vicinity of the positioning bumps 12B. Hence, the positioning bumps 12B can be discriminated from the general bumps 12. The resin layer 13 can be processed to define the positioning bumps 12B by, for example, laser beam projection, eximer laser, etching, mechanical polishing or blasting, these means being also used in the aforementioned protruding electrode exposing step. Hence, there is no need to greatly modify the fabrication facility for resin processing.

A description will be given of a method of discriminating the positioning bumps 12B from the general bumps 12. Fig. 50(C) is an enlarged view of a

part of the positioning bump 12B, and Fig. 50(D) is a top view of the positioning bump 12B. Fig. 51(A) is an enlarged view of the general bump 12, and Fig. 51(B) is a top view of the general bump 12.

As described previously, the positioning bump 12B has the same structure as that of the general bump 12. Hence, it is impossible to discriminate the general bump 12 and the positioning bump 12B only by referring to their structures themselves. The bumps 12 and 12B have a spherical shape or a rugby ball shape, and thus the diameters thereof viewed from the top are different from each other due to the depths in which the bumps 12 and 12B are embedded in the resin layer 13.

More particularly, the general bump 12 is deeply embedded in the resin layer 13, and thus a comparatively small diameter L2 of the exposed portion can be observed when viewing the general bump 12 from the top, as shown in Fig. 51(B). In contrast, the positioning bump 12B is greatly exposed from the resin layer 13 by the aforementioned resin process, and thus a comparatively large diameter L1 of the exposed portion can be observed when viewing the positioning bump 12 from the top, as shown in Fig. 50(D) ($L1 > L2$).

Hence, it is possible to discriminate the general bump 12 and the positioning bump 12B from each other by measuring the diameters of the bumps 12 and 12B observed when viewing these bumps from the top. Hence, it is possible to position the semiconductor device by referring to the positioning bumps 12B.

A description will be given of a method for mounting the semiconductor device fabricated by any of the foregoing embodiments of the present invention.

Fig. 52 shows a first embodiment of the mounting method. Fig. 52(A) shows a method for mounting the semiconductor device 10 fabricated by the

method according to the aforementioned first embodiment of the present invention, wherein the bumps 12 are bonded to the mounting board 14 by using bonding members 125 such as solder paste. Fig. 52(B) shows a method for mounting a semiconductor device 10G fabricated by the method according to the aforementioned fourteenth embodiment, wherein the straight bumps 18 are bonded to the mounting board 14 by using the bonding members 125 such as solder paste. Fig. 52(C) shows a method for mounting a semiconductor device 10H fabricated by the method according to the aforementioned fifteenth embodiment, in which the external connection terminals 90 provided to the ends of the bumps 12 are bonded to the mounting board 14.

Fig. 53 shows a second embodiment of the mounting method. The mounting method shown in Fig. 53 mounts the semiconductor device 10 on the mounting board 14 and arranges an under fill resin126.

Fig. 53(A) shows an arrangement in which the bumps 12 of the semiconductor device 10 are directly bonded to the mounting board 14 and then the under fill resin 126 is provided. Fig. 53(B) shows an arrangement in which the bumps 12 are bonded to the mounting board 14 through the bonding members 125, and then the under fill resins 126 are provided.

As described above, the semiconductor devices 10, 10A - 10H have the arrangements in which the resin layers 13, 13A and 13B are formed on the substrates 16, which are definitely protected thereby.

On the other hand, the portions of the bumps 12, 18 and 90 bonded to the mounting board 14 are exposed and may be oxidized. Also, if there is a large difference in thermal expansion ration between the mounting board 14 and the substrate 16, a large magnitude of stress may be applied to the bonded portions of the bumps 12, 18 and 90 and the mounting board 14. With the above in mind, the under fill

bumps, but executes the resin sealing step immediately after a semiconductor element forming step is performed. In the semiconductor element forming step, given electronic circuits are formed on the surface of the substrate 16, and the lead lines 96 and the connection electrodes 98 are formed thereon, as has been described with reference to Fig. 40. Further, in the present step, the external connection electrodes 140 are formed on the connection electrodes 98.

Fig. 59 shows the substrate in a state in which the semiconductor element forming step is completed. As shown in this figure, the external connection electrodes 140 are arranged along an edge of each of the rectangular areas (depicted by the solid lines), which correspond to respective semiconductor elements.

After the substrate forming step is carried out, a resin sealing step is carried out, in which the substrate 16 is loaded onto the mold and the resin 13 is compression-molded. The present resin sealing step is the same as that of the aforementioned first embodiment, and a description thereof will be omitted.

When the resin sealing step is completed, the resin layer 13 is formed on the entire surface of the substrate 16. Hence, the lead lines 96 and the connection electrodes 98 are covered by the resin layer 13. After the resin sealing step, a separating step is immediately carried out rather than the protruding electrode exposing step because the bumps are not formed.

The present embodiment is characterized by cutting, in the separating step, the substrate 16 in the position where the external connection electrodes 140 are formed. In Fig. 59, the broken lines denote the cutting positions. The substrate 16 is cut in the cutting position together with the resin layer 13, parts of the external connection electrodes 140 are

cut, so that the semiconductor devices 10J can be obtained in which the external connection electrodes 140 are laterally exposed at the interface between the substrate 16 and the resin layer 13.

As described above, the fabrication method of the present embodiment does not need the bump forming step and the protruding electrode exposing step, which are required in the aforementioned embodiments. Further, the external connection electrodes 140 can be exposed from the resin layer 13 by merely cutting the substrate 16 in the cutting positions together with the resin layer 13. Hence, the semiconductor devices 10J can easily be fabricated.

A description will now be given, with reference to Figs. 60 through 62, of a method for fabricating a semiconductor device according to a twenty ninth embodiment of the present invention. The present fabrication method is directed to fabricating the semiconductor device 10J shown in Fig. 63. In Figs. 60 through 62, parts that have the same structures as those shown in Fig. 59 are given the same reference numbers and a description thereof will be omitted.

As described previously, the twenty eight embodiment fabrication method described with reference to Fig. 59 can fabricate the semiconductor device 10J with ease. However, the separating step is required to cut the substrate 16 not only at the positions indicated by the broken lines shown in Fig. 59 but also at the positions indicated by the solid lines shown therein. Further, parts indicated by arrows W are unnecessary (and discarded). Hence, the twenty eighth embodiment method does not execute the cutting process efficiently in the separating step and does not substrate 16 efficiently.

Fig. 60 shows the substrate 16 in a state in

metallic films 173 cooperate with each other and function as the solder bumps of the BGA type semiconductor device. Hence, the mounting performance can be improved.

The method for fabricating the semiconductor device 170 will be described with reference to Figs. 72 and 73. Lead frame 180 shown in Fig. 72 is prepared. The lead frame 180 is made of, for example, copper (Cu). A plurality of recess portions 181 having a counterpart shape of the resin projections 177 are formed in the positions corresponding to those of the resin projections 177. The metallic films 173 are formed on the surfaces of the recess portions 181.

First, the semiconductor elements 171 are mounted on the lead frame 180. Next, the lead frame 180 are loaded to a wire bonding apparatus, which arranges the wires 178 between the electrode pads 174 of the semiconductor elements 171 and the metallic films 173 formed on the lead frame 180. Hence, the semiconductor elements 171 and the metallic films 173 are electrically connected. Fig. 72 shows the arrangement observed after the above steps are completed.

After the wires 178 are arranged, the resin package 172 is formed on the lead frame 180 so as to seal the semiconductor elements 171. In the present embodiment, the resin package 172 is formed by the compression-molding. Fig. 73 shows the lead frame 180 on which the resin package 172 is formed.

After the resin package 172 is formed, the arrangement is cut at the position indicated by the broken lines shown in Fig. 73, and then a removing step is carried out in which the resin package 172 is removed from the lead frame 180. Thus, the semiconductor device 170 can be obtained. In the removing step, the lead frame 180 is placed in an etchant and is thus dissolved. The etchant used in

the removing step is required to dissolve the lead frame 180 only and not to dissolve the metallic films 173.

Since the lead frame 180 is totally dissolved, the resin package 172 is separated from the lead frame 180. The metallic films 173 are disposed to the resin projections 177, and thus the semiconductor device 170 shown in Fig. 71 can be obtained. Hence, the above method makes it possible to definitely remove the lead frame 180 from the resin package 172 with ease and to improve the yield.

The semiconductor device 170A shown in Fig. 74 has an arrangement in which the semiconductor elements 171 are arranged in the single resin package 172. Hence, the semiconductor device 170A can be made to have multiple functions. The method for fabricating the semiconductor device 170A is almost the same as that which has been described with reference to Figs. 72 and 73, while there is an only minor difference such that the cutting positions indicated in Fig. 75(B) are different from those in the previously described method. Hence, a detailed description of the method for fabricating the semiconductor device 170A will be omitted.

Figs. 78 through 80 show a method for fabricating a semiconductor device according to a thirtieth embodiment of the present invention. First, a semiconductor device 210 fabricated by the thirtieth embodiment will be described by referring to Fig. 78. In the following description, semiconductor devices having a T-BGA (Tape-Ball Grid Array) structure will exemplarily be described. However, the present invention can be applied to semiconductor devices of other BGA structures.

The semiconductor device 210 is generally made up of a semiconductor element 211, a wiring board 212, a frame 213, protruding electrodes 214 and a

are connected thereto.

The insulating film 219 is an insulating resin film such as polyimide, and connection holes 219a are formed therein in positions corresponding to the positions of the protruding electrodes 214. The leads 218 and the protruding electrodes 214 are electrically connected through the connection holes 219a. The insulating film 219 protrudes from the leads 218.

The frame 213 is formed of a metallic substance such as copper or aluminum. In the central portion of the frame 213, a cavity 223 is formed so as to face the attachment hole 217a formed in the base film 217. In the present embodiment, the cavity 223 penetrates the frame 213 and connects the upper and lower surfaces thereof. The frame 213 has a rectangular shape when viewing it from the top. Hence, the cavity 223 forms the frame 213 into a rectangular frame shape.

The aforementioned wiring board 212 having flexibility is bonded to and fixed to the lower surface of the frame 213 by an adhesive 222. In the state in which the wiring board 212 is arranged to the frame 213, the inner lead portions 220 of the leads 218 extend into the cavity 223. The semiconductor element 211 is bonded, in flip-chip bonding formation, to the inner lead portions 220 extending into the cavity 223. Hence, the semiconductor element 211 is located within the cavity 223.

The outer lead portions 221 of the leads 218 are disposed so as to be located at the lower surface side of the frame 213. The protruding electrodes 214 are arranged to the outer lead portions 221. In the present embodiment, the protruding electrodes 214 are formed of solder bumps, and are bonded to the outer lead portions 221 via the connection holes 219a formed in the insulating film 219 by using solder balls.

the protruding electrode forming step, the element mounting step and the testing step can be executed by using the known techniques. The present method has a unique feature in the resin sealing step, which will mainly be described below.

Fig. 79 shows the resin sealing step used in the thirtieth embodiment.

As shown in Fig. 79, the resin sealing step commences loading, onto a mold 224 for fabricating semiconductor devices (hereinafter simply referred to as mold), the wiring board 212 on which the semiconductor element 211 is mounted through the semiconductor element forming step, the wiring board forming step and the element mounting step.

The structure of the mold 224 will be described. The mold 224 is generally made up of an upper mold 225 and a lower mold 226, which are respectively equipped with heaters that are not shown. The heaters heat and melt sealing resin before molding (the sealing resin before molding is specifically indicated by a reference number 227).

The upper mold 225 is elevated in directions Z1 and Z2 indicated by an arrow by means of an elevating apparatus, which is not shown. The lower surface of the upper mold 225 is a cavity surface 225a, which is flat. The upper mold 225 has a very simple shape, which can be produced at a less-expensive cost.

The lower mold 226 is made up of a first lower mold half body 228 and a second lower mold half body 229. The first lower mold half body 228 is arranged within the second lower mold half body 229. The upper and lower mold half bodies 228 and 229 can independently be elevated in the directions Z1 and Z2 indicated by the arrow by means of the elevating apparatus which is not shown.

In the present embodiment, a resin film 231

the wiring board 212 from being broken and to realize the highly reliable resin sealing process.

In the resin sealing step, if the first lower mold half body 228 is moved too fast, the molding pressure is abruptly increased, so that the connecting portions between the bump electrodes 216 and the inner lead portions 220 may be damaged. If the first lower mold half body 228 is moved too slowly, the molding pressure becomes too low, so that some portions may not be filled with resin and the time necessary to execute the resin sealing step may become long. The fabrication efficiency is degraded. With the above in mind, the moving speed of the first lower mold half body 228 is selected to an appropriate level at which the above contradictory problems do not occur.

After the sealing resin 215 is formed, the step of removing the wiring board 212 from the molding resin 224 is carried out. In order to remove the wiring board 212 from the mold 224, the first lower mold half body 228 is moved down in the direction Z1. Since the resin film 231 having a good detachment performance is provided to the cavity surface of the first lower mold half body 228, the first lower mold half body 228 can easily be removed from the sealing resin 215.

After the first lower mold half body 228 is removed from the sealing resin 215, the upper mold 225 and the second lower mold half body 229 are moved so as to become away from each other. Hence, the wiring board 212 can be taken out of the mold 224. There is no problem even when the first lower mold half body 228 is moved at the same time as the second lower mold half body 229 and the upper mold 225 are moved.

After the wiring board 212 is removed from the mold 224, the protruding electrodes 214 are formed on the wiring board 212. The protruding electrodes

semiconductor device according to the thirty first embodiment of the present invention.

Fig. 81 shows a semiconductor device 210A according to the thirty first embodiment of the present invention. In Fig. 81, parts that have the same structures as those of the semiconductor device 10 according to the thirtieth embodiment of the present invention are given the same reference numbers, and a description thereof will be omitted.

The semiconductor device 210A according to the present embodiment is characterized by providing a heat radiating plate 233 to the mounting-side surface (the lower surface in the figure) of the sealing resin 215. The heat radiating plate 233 is formed of a metal having a good heat radiating performance such as aluminum. By providing the heat radiating plate 233 to the sealing resin 215 sealing the semiconductor element 211, it is possible to efficiently radiate heat generated in the semiconductor element 211. Hence, it is possible to suppress the temperature of the semiconductor element 211 from raising and to thus improve the reliability in the operation of the semiconductor device 210A.

The semiconductor device 210A according to the present embodiment has the wiring board 212 arranged in a direction different from that of the semiconductor device 210 according to the aforementioned thirtieth embodiment. That is, the base film 217 forms the lowermost layer, and the leads 218 and the insulating film 219 are arranged in a stacked formation on the base film 217.

Hence, the insulating film 219 is bonded to the frame 213 by the adhesive 222, and the connection holes 217b accommodating the protruding electrodes 214 are formed on the base film 217. As described above, the wiring board 212 can be arranged in any of the two different directions by selecting the positions in

semiconductor device 210A equipped with the heat radiating plate 233.

The resin sealing step shown in Fig. 83 is characterized by arranging the heat radiating plate 233 to the cavity surface 230 of the first lower mold half body 228 and arranging a resin film 232 having a good detachability to the cavity surface 225a of the upper mold 225.

Hence, the present embodiment resin sealing step easily fabricates the semiconductor device 210A equipped with the heat radiating plate 233 and easily detaches the sealing resin 215 from the cavity surface 225a of the upper mold 225.

A description will now be given of a semiconductor device according to a thirty second embodiment of the present invention.

Fig. 84 shows a semiconductor device 210B according to the thirty second embodiment of the present invention. In Fig. 84, parts that have the same structures as those of the semiconductor device 210 according to the thirtieth embodiment are given the same reference numbers, and a description thereof will be omitted.

The semiconductor device 210B according to the present embodiment is characterized by providing the first heat radiating plate 233 to the mounting-side surface (the lower surface in the figure) of the sealing resin 215 as in the case of the semiconductor device 210A according to the thirty first embodiment and by providing a second heat radiating plate 234 to the upper surface of the frame 213.. The second heat radiating plate 234 is made of a metal having a good heat radiating performance such as aluminum as in the case of the first heat radiating plate 233.

The heat radiating plates 233 and 234 are arranged so as to sandwich the semiconductor element 211, and more efficiently radiate heat generated in

210B according to the thirty second embodiment are given the same reference numbers and a description thereof will be omitted.

The semiconductor device 210D is characterized by placing the semiconductor element 211 on a wiring board 212A so that protruding electrodes 214 can be arranged below the semiconductor element 211. The wiring board 212 is different from those of the semiconductor devices 210 - 210C in that there are no attachment holes 217a.

The above arrangement increases the degree of freedom in arrangement of the protruding electrodes 214 and realizes down-sized semiconductor device 210D. The sealing resin 215 of the semiconductor device 210D can be formed by the compression-molding process.

A description will now be given, with reference to Fig. 87, of a resin sealing step. In Fig. 87, parts that have the same structures as those of the mold 224 described with reference to Fig. 79 are given the same reference numbers, and a description thereof will be omitted.

A mold 224A used in the present embodiment is generally made up of the upper mold 225 and a lower mold 226A. The mold 224A has a multi-process arrangement which is capable of totally processing a plurality of (two in the present embodiment) sealing resins 215.

The upper mold 225 is almost the same as that of the mold 224 shown in Fig. 79. However, the mold 224A has a comparatively large size because it has the multi-process arrangement. The lower mold 226A is made up of first and second lower mold half bodies 228 and 229A. Two first lower mold half bodies 228 are arranged in the second lower mold half body 229.

An excess resin removing mechanism 240 for removing excess resin is provided in the central

After the wiring board 212 is clamped between the upper body 225 and the lower mold 226A, the first lower mold half bodies 228 are driven to move up in the direction Z2. Hence, the resins 227 are compressed and molded in the cavity portions 239. In order to definitely seal the semiconductor elements 211, it is required to set the movement speed of the first lower mold half bodies 228 to an appropriate level. In other words, the appropriate level setting of the movement speed of the first lower mold half bodies 228 leads to the appropriate level setting of the compression pressure applied to the sealing resins 227 in the cavity portions 239.

According to the present embodiment, the compression pressure applied to the sealing resins 227 can be controlled not only by controlling the movement speed of the first lower mold half bodies 228 but also controlling the movement speed of the pressure control rod 243 of the excess resin removing mechanism 240. More particularly, when the pressure control rod 243 is moved down, the pressure applied to the sealing resins 227 is reduced. When the pressure control rod 243 is moved up, the pressure applied to the sealing resins 227 is increased.

For example, if the amounts of the resins 227 are greater than the volumes of the sealing resins 215, and excess resins increase the pressures of the cavity portions 239, the resin layers may not be formed appropriately. In this case, the pressure control rod 243 is moved down in the direction Z1, and excess resins are transferred to the pot portions 242 through the openings 241. Hence, even if there is an excess amount of resin, the pressures in the cavities 239 can be maintained at the appropriate level.

As described above, the excess resin removing mechanism 240 functions to remove excess resin generated in the step of forming the sealing

sized, as compared to the semiconductor device 210 of the thirtieth embodiment in which the protruding electrodes 214 are arranged on the lower surface of the frame 213.

A description will be given of a method for fabricating the above semiconductor device 210E. First, the wiring board 245 as shown in Figs. 89(A) and 103 is prepared. The wiring board 245 has a rectangular base portion 251 on which the semiconductor element 211 to be mounted, and the extending portions 246 arranged on the four sides of the base portion 251.

An attachment hole 248 (shown in Fig. 103) for mounting the semiconductor element 211 is formed in the central position of the base portion 251. Leads 218 are provided between edge portions of the attachment hole 248 and lands 249 formed in the extending portions 246 and located in the positions in which the protruding electrodes 214 are to be provided. The extending portions 246 have a trapezoidal shape in order to prevent the adjacent extending portions 246 from contacting each other when the wiring board 245 is bent.

The leads 219 are protected by the insulating film 219 (see Fig. 90(E)). The portions of the insulating film 219, which are located in the positions in which the lands 249, that is, the protruding electrodes 214 are to be provided, are removed so that the leads 218 are exposed. Fig. 103 shows an enlarged view of the wiring board 245 shown in Fig. 89(A).

The semiconductor element 211 is bonded to the upper surface of the wiring board 245 in the flip-chip bonding formation, and the frame 213 is bonded thereto by the adhesive 222. The frame 213 used in the present embodiment has a size smaller than that of the frame used in the thirtieth embodiment because the

extending portions 246 are bent in the directions indicated by the arrows, and the bent extending portions 246 are bonded to the upper surface of the frame 213 by a second adhesive 247.

Fig. 90(G) shows the wiring board 245 observed after the bending step is completed. By the step of bending the extending portions 246 so as to be located on the upper surface of the frame 213, the lands 249 on which the protruding electrodes 214 are to be provided are located on the upper portion of the frame 213.

Then, a protruding electrode forming step is executed so that the protruding electrodes 214 are formed on the lands 249 on the upper portion of the frame 213 by, for example, the transfer method. Hence, the semiconductor device 210E is obtained. The method of fabricating the semiconductor device 210E forms the sealing resin 215 by using the compression molding as in the case of the fabrication method of the thirtieth embodiment, and improves the reliability of the device 210E. The process for providing the extending portions 246 on the upper surface of the frame 213 can easily be obtained by merely bending the extending portions 246.

A description will be given of a semiconductor device and its fabrication method according to the thirty sixth embodiment of the present invention. Fig. 91 shows a semiconductor device 210F and its fabrication method according to the thirty sixth embodiment of the present invention. In Fig. 91, parts that have the same structures as those shown in Figs. 88 through 90 are given the same reference numbers and a description thereof will be omitted.

Fig. 91(D) shows the semiconductor device 210F according to the thirty sixth embodiment of the present invention. The semiconductor device 210F has

connection holes 217b are opened downwards. Then, the protruding electrodes 214 electrically connected to the leads 218 are formed in the connection holes 217b by the transfer method or the like. Hence, the semiconductor device 210H shown in Fig. 93(D) can be obtained.

The semiconductor device 210H thus obtained has the extending portions 246 located below the heat radiating plate 233, so that the semiconductor element 211 is exposed to the outside. Hence, heat generated in the semiconductor element 211 can efficiently be radiated, and the semiconductor device 210H has improved heat radiating performance.

The extending portions 246 of the semiconductor device 210H are bent and the protruding electrodes 214 are provided thereon. Hence, the semiconductor device 210H can be down sized.

A description will be given of a semiconductor device and its fabrication method according to the thirty ninth embodiment of the present invention. In Fig. 94, parts that have the same structures as those shown in Figs. 88 through 90 are given the same reference numbers, and a description thereof will be omitted.

Fig. 94(D) shows a semiconductor device 210I according to the thirty ninth embodiment of the present invention. The semiconductor device 210I has the same structure as the semiconductor device 210H according to the thirty eighth embodiment of the present invention. The method for fabricating the semiconductor device 210I differs from that for fabricating the semiconductor device 210H in that the second adhesive 247 is provided to the heat radiating plate 233 rather than the wiring board 245, as shown in Figs. 94(A) and 94(B). That is, the second adhesive 247 may be provided to the wiring board 245 or the heat radiating plate 233.

semiconductor device and its fabrication method according to a forty first embodiment of the present invention. Fig. 96 shows a semiconductor device 210K and its fabrication method according to the forty first embodiment of the present invention. In Fig. 96, parts that have the same structures as those shown in Figs. 84, and 88 through 90 are given the same reference numbers, and a description thereof will be omitted.

Fig. 96(D) shows the semiconductor device 210K according to the forty first embodiment of the present invention. The semiconductor device 210K has a structure similar to that of the semiconductor device according to the thirty second embodiment described with reference to Fig. 84 and is, more particularly, characterized by providing a second heat radiating plate 234 to the upper surface of the frame 213. The second heat radiating plate 234 is formed of a metal having a good heat radiating performance such as aluminum as in the case of the first heat radiating plate 233.

The heat radiating plates 233 and 234 are provided so as to sandwich the semiconductor element 211, so that heat generated in the semiconductor element 211 can efficiently be radiated. Thus, the semiconductor device 210K has improved reliability.

The semiconductor device 210K can be fabricated as follows. The semiconductor device 210K employs wires 235 as means for connecting the semiconductor element 211 and the wiring board 245. Hence, the second heat radiating plate 234 is bonded to the upper surface of the frame 213 by, for example, an adhesive so that these components are unified. Hence, a bottom portion defined by the second heat radiating plate 234 is defined in the cavity 223 formed in the frame 213.

Then, the semiconductor element 211 is

same structures as those shown in Figs. 88 through 90 and 96 are given the same reference numbers, and a description thereof will be omitted.

Fig. 97(D) shows the semiconductor device 210L according to the forty second embodiment of the present invention. The semiconductor device 210L has an arrangement in which the second heat radiating plate 234 is provided to the upper surface of the frame 213, as in the case of the semiconductor device 210K according to the forty first embodiment. The semiconductor device 210L has the wiring board 245 arranged by turning the wiring board 245 of the semiconductor device 210K upside down.

That is, as shown in Fig. 97(A), the wiring board 245 has the base film 217, the leads 218 and the insulating film 219 stacked in that order from the lowermost layer side. Even by turning the wiring board 245 upside down, the same effects as those of the semiconductor device 210K can be obtained.

The extending portions 246 of the semiconductor device 210L are bent towards the second heat radiating plate 234. The present embodiment does not necessarily require the insulating film 219, which can be omitted when the frame 213 and the adhesives 222 and 247 are formed of substances having electrically insulating performance.

Fig. 98(D) shows the semiconductor device 210M according to the fourth third embodiment of the present invention. The semiconductor device 210M has an arrangement in which the second heat radiating plate 234 is provided on the upper surface of the frame 213 as in the case of the semiconductor device 210K. However, the semiconductor device 210M is characterized in that the extending portions 246 are bent towards the heat radiating plate 233 in contrary to the semiconductor devices 210K and 210L. The method of bending the extending portions 246 and

obtained.

A description will now be given of semiconductor devices and fabrication methods thereof according to forty fifth and forty sixth embodiments of the present invention. Fig. 100 is a diagram showing a semiconductor device 210P and its fabrication method according to the forty fifth embodiment of the present invention. Fig. 101 is a diagram showing a semiconductor device 210Q and its fabrication method according to the forty sixth embodiment of the present invention. In Figs. 100 and 101, parts that have the same structures as those shown in Figs. 88 through 90 and 99 are given the same reference numbers, and a description thereof will be omitted.

Fig. 100(D) shows the semiconductor device 210P according to the forty fifth embodiment of the present invention. The semiconductor device 210P has an arrangement in which the bottom portion 237 is integrally formed in the frame 213A as in the case of the semiconductor device 210N according to the forty fourth embodiment. The semiconductor device 210P has the wiring board 245 obtained by turning the wiring board 245 of the semiconductor device 210N upside down.

That is, as shown in Fig. 100(A), the wiring board 245 has the base film 217, the leads 218 and the insulating film 219 stacked in that order from the lowermost layer side. The semiconductor device 210P has the same effects as those of the semiconductor device 210N even by turning the wiring board 245 upside down. The extending portions 246 are bent towards the upper side of the frame 213A. The present embodiment does not necessarily require the insulating layer 219, which can be omitted by forming the frame 213A and the adhesives 222 and 247 of electrically insulating substances.

description thereof will be omitted.

Fig. 47(F) shows the semiconductor device 210R according to the forty seventh embodiment of the present invention. The frame 213A of the semiconductor device 210R has the same structure as that of the semiconductor device 210N described with reference to Fig. 99. That is, the frame 213A has the integrally formed bottom portion 237.

A wiring board 245A used in the present embodiment is different from the wiring board 245 shown in Figs. 89(A) and 103 in that the wiring board 245A does not have the attachment hole 248 for attaching the semiconductor element 211. An enlarged view of the wiring board 245A employed in the semiconductor device 210R is shown in Fig. 106.

As shown in this figure, lands 249 are provided on a base portion 251A of the wiring board 245A. Connection electrodes 253, which are to be wire-bonded to the semiconductor element 211 are provided in outer edge portions of the extending portions extending to four peripheral edges of the base portion 251A. The connection electrodes 253 and the lands 249 are electrically connected by the leads 218 formed on the extending portions 246 and the base portion 251.

As shown in Fig. 102(A), the base portion 251A is positioned on the bottom portion 237 of the frame 213A, and the wiring board 245A is positioned on the bottom portion 237 by an adhesive (not shown). In this state, the extending portions 246 extend further out than the external periphery of the frame 213A. The semiconductor element 211 is mounted in the cavity 223A formed in the frame 213A. An adhesive 247A for fixing the extending portions 246 to the frame 213A is provided to the lower surface of the frame 213A.

After the base portion 251A of the wiring board 245A is fixed to the bottom portion 237 of the

frame 213A, a step of bending the extending portions 246 is carried out without execution of the resin sealing step employed in the aforementioned embodiments. More particularly, as indicated by the arrows in Fig. 102(B), the extending portions 246 are bent and are then fixed to the frame 213A by the adhesive 247A.

Thus, as shown in Fig. 102(C), the connection electrodes 253 formed on the extending portions 246 become close to the semiconductor element 211. Then, the wires 235 are provided between the connection electrodes 253 and the semiconductor element 211 by the wire bonding process. Fig. 102(D) shows a state in which the wires 235 are provided between the connection electrodes 253 and the semiconductor element 211.

According to the present embodiment, a resin sealing step of forming the sealing resin 215 is carried out after the step of bending the extending portions 246 and the wire bonding step of bonding the wires 235. Fig. 102(E) shows the wiring board 245A to which the sealing resin 215 is provided. The resin sealing step can be carried out by using the aforementioned mold 224, so that the sealing resin 215 is formed by the compression molding process. In the present embodiment, the heat radiating plate 233 is provided at the same time as the sealing resin 215 is formed (see Fig. 82).

After the sealing resin 215 is formed, the protruding electrodes 214 are formed on the lands 249 by, for example, the transfer method. Thus, the semiconductor device 210R shown in Fig. 102(F) can be obtained. In the semiconductor device 210R thus fabricated, the protruding electrodes 214 are positioned at the side of the bottom portion 237 of the frame 213A, and the cavity 223A is not formed in these positions. Hence, the whole area of the bottom

210E through 210R.

A wiring board 245C shown in Fig. 105 is of a type in which the semiconductor element 211 are bonded to the leads by the wiring bonding method (hereinafter referred to as a wire connection type). Hence, the wiring board 245C differs from the wiring boards 245 and 245A of the TAB type shown in Figs. 103 and 104 in that the inner lead portions 220 do not protrude within the loading hole 248. The wiring board 245A shown in Fig. 106 has been described previously, and a description thereof will be omitted here.

A wiring board 245D shown in Fig. 107 is of the TAB type, and is characterized in that each of the extending portions 246A has a triangular shape. Hence, pads 249 can be arranged along slant edges of the triangular shape. Hence, the adjacent pads 249 (that is, the protruding electrodes 214) can be arranged at a comparatively wide pitch. Thus, the pads 249 can easily be formed, and no problem will occur even if it is required to arrange an increased number of protruding electrodes 214. The extending portions 246A shown in Fig. 107 have a triangular shape, but are not limited thereto. That is, the extending portions 246A can be formed in an arbitrary shape which makes it possible to arrange the pads 249 at a wide pitch.

A wiring board 245E shown in Fig. 108 is of the TAB type, and is characterized in that the extending portions 246A have a triangular shape and the base film 217 does not have any portion that is to be bent. The wiring board 245E in the present embodiment makes it possible to prevent the wiring board 245E from flaking off from the frames 213, 213A and the heat radiating plates 233 and 234, so that the semiconductor device can be down sized and the reliability thereof can be improved. Further, the

connection electrodes 253 makes it possible to widen the area of each of the connection electrodes 253 and to simplify the wire bonding process (electrical connection process) for making connections to the semiconductor element 211.

The curved corner portions 253a of the connection electrodes 253 function to decentralize stress generated when a bonding tool (ultrasonic welding tool) used for bonding the wires 235 and the connection electrodes 253. Hence, the electrical connections between the wires 235 and the connection electrodes 253 can definitely be made.

A description will now be given, with reference to Figs. 111 through 113, of a semiconductor device and its fabrication method according to a forty eighth embodiment of the present invention. In Figs. 111 through 113, parts that have the same structures as those of the semiconductor device 210E according to the thirty fifth embodiment shown in Figs. 88 through 90 are given the same reference numbers, and a description thereof will be omitted.

Fig. 111 shows a semiconductor device 210S according to the forty eighth embodiment of the present invention, and Figs. 112 and 113 show a method for fabricating the semiconductor device 210S. The semiconductor device 210S is characterized by using mechanical bumps 255 as protruding electrodes. The mechanical bumps 255 are obtained by deformation-processing or plastic-deforming leads 218 formed in the wiring board 245J, so that the deformed portions of the leads 218 protrude from the surface of the wiring board 245J and thus serve as protruding electrodes.

The use of the mechanical bumps 255 does not need ball members necessary for the transfer method employed in the aforementioned embodiments. Hence, the number of components can be reduced and the

fabrication process can be simplified. The deformation-processing step requires a simple step of, for example, pressing the leads 218 by a punch (tool) or the like. Hence, the mechanical bumps 255 (protruding electrodes) can easily be formed at low cost.

A description will be given of the method for fabricating the semiconductor device 210S. Fig. 112(A) shows the wiring board 245J in which the mechanical bumps 255 are formed after the resin sealing step is executed. As shown in this figure, the mechanical bumps 255 are formed in the extending portions 246 of the wiring board 245J.

An enlarged view of a portion indicated by an arrow A shown in Fig. 112(A) is shown in Figs. 112(B) through 112(D). As shown in these figures, the mechanical bumps 255 can have various structures.

Mechanical bumps 255A shown in Fig. 112(B) are characterized as follows. The leads 218 are pressed (deformation processing) integrally with the insulating film 219. Thereby, the pressed and deformed portions of the leads 218 and the insulating film 219 protrude from the connection hole 217b. Further, cores 256 are provided to resultant recess portions formed on the back surface of the deformed portions. Thus, the cores 256 have a shape which corresponds to the recess portions formed in the back surfaces of the mechanical bumps 255.

The insulating film 219 is subjected to the deformation processing together with the leads 218, and is not required to be removed. Hence, the step of forming the mechanical bumps 255A is simple. Further, the cores 256 arranged in the recess portions prevent the mechanical bumps 255A from being deformed even when the mechanical bumps 255A receives a pressure at the time of mounting the semiconductor device 210S.

In the structure shown in Fig. 112(C),

112(A) can be obtained. Then, a bending step is performed as shown in Fig. 113, and the extending portions 246 are bent towards the upper surface of the frame 213 and is fixed thereto by the second adhesive 247. Thus, the semiconductor device 210S shown in Fig. 111 can be obtained.

Fig. 114 shows a semiconductor device 210T and its fabrication method according to a forty ninth embodiment of the present invention. The semiconductor device 210S and its fabrication method described with reference to Figs. 111 through 113 employ the flip-chip bonding in order to connect the semiconductor element 211 and the wiring board 245J.

In contrast, as shown in Fig. 114, the forty ninth embodiment is characterized by connecting the semiconductor element 211 and the wiring board 245J by the wires 235. Even when the mechanical bumps 255 are employed, the semiconductor element 211 and the wiring board 245J can be connected by the TAB method or the wire bonding method. The semiconductor device 210T and its fabrication method are the same as the semiconductor device 210S and its fabrication method described with reference to Figs. 111 through 113 except for the arrangement of the connections between the semiconductor element 211 and the wiring board 245J, and thus a description thereof will be omitted.

A description will be given of a semiconductor device and its fabrication method according to a fiftieth embodiment of the present invention. Fig. 115 is a diagram showing a semiconductor device 210U and its fabrication method according to the fiftieth embodiment of the present invention. In Fig. 115, parts that have the same structures as those shown in Fig.s 102, 111 and 112 are given the same reference numbers, and a description thereof will be omitted.

Fig. 115(F) shows the semiconductor device

210U according to the fiftieth embodiment of the present invention. The frame 213A used in the semiconductor device 210U has the same structure as that of the semiconductor device 210R described with reference to Fig. 102. That is, the frame 213A includes the integrally formed bottom portion 237. A wiring board 245K used in the present embodiment has an arrangement in which the protruding electrodes 255 are formed on base portion 251A.

As shown in Fig. 115(A), the base portion 251A is positioned on the bottom portion 237 of the frame 213A, and is fixed thereto by the second adhesive 247. The extending portions 246 extend outwards from the outer periphery of the frame 213A. The semiconductor element 211 is mounted by the adhesive 236 within the cavity 223A formed in the frame 213A.

After the base portion 251A of the wiring board 245A is fixed to the bottom portion 237 of the frame 213A, the extending portions 246 are bent as shown in Fig.s 115(B) and 115(C), and the extending portions 246 are fixed to the frame 213A by the adhesive 247A. Then, the wires 235 are provided between the connection electrodes 253 and the semiconductor element 211 by the wire bonding method. Fig. 115(D) shows a state in which the wires 235 are provided between the connection electrodes 253 and the semiconductor element 211.

After the wires 235 are provided, a resin sealing step is performed. Fig. 115(E) shows a state in which the wiring board 245K is loaded onto the mold 224C. In the present embodiment, the mechanical bumps 255 are formed on the wiring board 245K preceding to the resin sealing step. Thus, inserting holes 257 into which the mechanical bumps 255 are inserted are formed in an upper mold 225B of the mold 224C.

The sealing resin 215 is shaped by the

semiconductor devices 210V - 210X shown in Fig. 116 other than the mechanical bumps 255 are the same as those of the aforementioned semiconductor devices 210A, 210B and 210D, and a description thereof will be omitted.

Fig. 117(E) shows a semiconductor device 210Y according to fifty first embodiment of the present invention, which is characterized in that the frame 213 or 213A used in the aforementioned embodiments is not used. Hence, the semiconductor element 211 is supported by only the sealing resin 215. Hence, it is possible to further facilitate down sizing of the semiconductor device 210Y and to reduce the fabrication cost and simplify the assembly work due to a reduction in the number of components.

A description will be given of a method for fabricating the semiconductor device 210Y. In the following description, the semiconductor device 210Y has the mechanical bumps 255 as protruding electrodes. However, the following method can be applied to semiconductor devices having protruding electrodes other than the mechanical bumps.

Fig. 117(A) shows a state in which the mechanical bumps 255 are already formed and a wiring board 246L to which the semiconductor element 211 is provided is loaded to the mold 224C. In the present embodiment, the semiconductor element 211 and the wiring board 246L are electrically connected together by the wires 235. The mold 224C has the inserting holes 257 into which the mechanical bumps 255 are inserted, as in the case shown in Fig. 115(E).

The wiring board 246L is loaded onto the mold 224C, and the upper mold 225B and the lower mold 226 are moved so as to be close to each other. Then, as shown in Fig. 117(B), the wiring board 246L is clamped between the upper mold 225B and the lower mold 226.

Then, as shown in Fig. 117(C), the first lower mold half body 228 is moved up, and the sealing resin 227 seals the semiconductor element 211 and the wire 235 with a predetermined compression pressure. That is, the sealing resin 215 is formed by the compression molding method. The resin sealing step is carried out in a state in which the heat radiating plate 233 is placed on the first lower mold half body 228. Hence, the heat radiating resin 215 can be provided at the same time as the sealing resin 215 is formed.

Fig. 117(D) shows a state in which the wiring board 245L to which the sealing resin 215 is provided is detached from the mold 224C. In this state, there are unnecessary extending portions 258 extending from the side portions of the sealing resin 215. The unnecessary portions 258 are cut and removed after the separating process, so that the semiconductor device 210Y shown in Fig. 117(E) can be obtained.

Fig. 118 shows a semiconductor device 310A according to a fifty fourth embodiment of the present invention. Fig. 118(A) shows a cross-sectional view of the semiconductor device 310A, and Fig. 118(B) is a side view of the semiconductor device 310A.

The semiconductor device 310A has a very simple structure, which is generally made up of a semiconductor element 312, an electrode board 314A, a sealing resin 316A and protruding terminals 318. The semiconductor device 312 (semiconductor chip) has a semiconductor substrate in which electronic circuits are formed. A plurality of bump electrodes 322 are formed on the mounting surface of the semiconductor element 312. The bump electrodes 322 has an arrangement in which solder balls are arranged by the transfer method, and are bonded to the electrode board 314 by the flip-flop bonding. Alternatively a reflow

plate 314 and parts of the protruding terminals 318. The sealing resin 316A is formed of resin having electrically insulating performance such as polyimide and epoxy, and a minimum size sufficient to cover and protect the semiconductor element 312. Hence, the down-sizing of the semiconductor device 310A can be realized.

In the state observed after the sealing resin 316A is formed, a back surface 328 of the semiconductor element 312 is exposed from the sealing resin 316A. There are no electronic circuits in the back surface of the semiconductor element 312, which has a comparatively large mechanical strength. Hence, there is no problem in the arrangement in which the back surface 328 is exposed from the sealing resin 316A. The above arrangement functions to improve the heat radiating performance of the semiconductor device 310A because heat generated in the semiconductor element 312 can be radiated from the back surface 328 to the outside.

In the state in which the sealing resin 316A is formed, the end portions of the electrode plate 314 are exposed from the side surfaces of the sealing resin 316A so that side terminals 320 can be formed. Hence, it is possible to use, together with the protruding terminals 318, side terminals 320 as external connection terminals for making connections to another board or device.

Fig. 128 shows a mounting arrangement of the semiconductor device according to the fifty fourth embodiment, and more particularly, shows a state in which the semiconductor device 310A is mounted on a mounting board 332. As shown in Fig. 128, the protruding terminals 418 are positioned between the bottom surface of the sealing resin 316A and the mounting board 332, and cannot be visually observed or connected to a test tool such as a probe from the

outside of the device.

The semiconductor device 310A has the side terminals 320 which are exposed from the side surfaces of the sealing resin 316A. Hence, even after the semiconductor device 312 is mounted on the mounting board 322, it is still possible to test the semiconductor device 310A by using the side t terminals 320. Hence, it is possible to detect a defective semiconductor device and to improve the yield and reliability.

Turning to Fig. 118 again, a further description will be given of the semiconductor device 310A.

The above-mentioned sealing resin 316A covers not only the semiconductor element 312 but also the interfaces at which the protruding terminals 318 of the electrode plate 314. Hence, the protruding terminals 318 are protected by the sealing resin 316A. Hence, it is possible to prevent the protruding terminals 318 from flaking off from the semiconductor device 310A due to external force. Since the sealing resin 316A has electrically insulating performance, it is possible to prevent the adjacent protruding terminals from being short-circuited particularly in an arrangement in which the protruding terminals 318 are arranged at a high density (that is, at a narrow pitch).

The protruding terminals 318 protrude from the sealing resin 316A. Hence, it is possible to definitely connect the protruding terminals 318 to the mounting board 332. Further, the semiconductor device 310A can be handled as in the case of the BGA (Ball Grid Array) as shown in Fig. 128. Hence, the mounting reliability can be improved.

The electrode plate 314A of the semiconductor device 310A will be drawn to attention.

As has been described previously, the

same structures as those shown in Fig. 118 are given the same reference numbers.

The fabrication method of the present embodiment includes an electrode plate forming step, a chip mounting step, a protruding terminal forming step, a sealing resin forming step and a cutting step. In the electrode plate forming step, a pattern forming process is carried out for a metallic base formed of a copper alloy (for example, a Cu-Ni-Sn system) which is generally used to form the lead frames. Thereby, a lead frame 324A having a plurality of electrode plates 314 is formed. The pattern forming process performed in the electrode plate forming step uses an etching method or press processing method.

The etching method and press processing method are generally used to form the lead frames. Hence, by applying the etching method or the press processing method to the step of forming the lead frames, the lead frame 324A can be formed without any increase in the facility.

Fig. 119(A) is a diagram of an enlarged view of a part of the lead frame 324A, in which four electrode plates 314A are depicted. According to the present embodiment fabrication method, a plurality of electrode plates 314A can be obtained from the lead frame 324A.

The electrode plates 314A have a plurality of metallic plate patterns 326, which can be processed to have arbitrary wiring patterns in the pattern forming step. Hence, the routing of wires can be realized by using the electrode plates 314A, so that the layout of external connection terminals formed on the electrode plates 314A can be determined with a large degree of freedom.

Fig. 119(B) shows a semiconductor element 312 (312A - 312C) provided on the electrode plates (the lead frame 324A). In the present embodiment,

three semiconductor elements 312A through 312C are mounted on a single electrode plate 314A. The semiconductor elements 312A - 312C are equipped with the bump electrodes 322 used for making electrical connections to the respective electrode plates 314A.

As shown in Fig. 119(B), the sizes of the semiconductor elements 312A - 312C may not be required to be equal to each other. The metallic plate patterns 326 formed on the electrode plates 314A are configured so as to correspond to the positions in which the bump electrodes 322 are to be formed.

After the electrode plate forming step is completed, the chip mounting step is performed, in which the semiconductor elements 312A through 312C are mounted on the electrode plates 314A and are electrically connected thereto. Figs. 120(A) and 120(B) show a state in which the semiconductor elements 312A - 312C are mounted on the respective electrode plates 314A.

The present embodiment employs the flip-chip bonding method as means for bonding the semiconductor elements 312A - 312C to the electrodes 314A so that the electrode plates 314A are directly bonded to the bump electrodes 322. Hence, it is possible to reduce the bonding areas between the semiconductor elements 312A - 312C and the electrode plates 314A and reduce the connection impedance.

After the chip mounting step is completed, the protruding terminal forming step is carried out, in which the protruding terminals 318 are formed in given positions of the metallic plate patterns 326 forming the electrode plates 314A. The protruding terminals 318 are formed of solder balls, which are bonded to the metallic plate patterns 326 by, for example, the transfer method. Fig. 121 shows the electrode plate 314A on which the protruding terminals 318 are arranged. The protruding terminals 318 are

board 332. As shown in this figure, the semiconductor device 310B is mounted on the mounting board 332 using solders 336 in a face-down formation. The solders 336 extend not only to the bottom portion of the electrode plate 314A but also to the side terminals 320, so that solder bonding can be realized.

The semiconductor device 310B can be mounted using the side terminals 320 only as in the case of a semiconductor device 310C of to a fifty sixth embodiment which will be described later. Hence, the semiconductor device 310B has an improved degree of freedom in mounting.

A description will now be given of a semiconductor device 310C according to the fifty sixth embodiment. More particularly, Fig. 124(A) shows a cross section of the semiconductor device 310B and Fig. 124(B) shows an upper surface thereof.

In the aforementioned semiconductor device 310B according to the fifty fifth embodiment, the side surface and side end portions of the electrode plate 314 are directly exposed from the sealing resin 316B. In contrast, the semiconductor device 310C is characterized in that only the side portions of the electrode plate 314A are exposed from the sealing resin 316C whereby the side terminals 320 can be formed.

The electrode plate 314A of the semiconductor device 310C is embedded in the sealing resin 316C while the side terminals 320 remain. Hence, it is possible to prevent the electrode plate 314A from flaking off from the sealing resin 316C due to thermal stress and external force and to thus improve the reliability of the semiconductor device 310C.

A description will now be given of a semiconductor device 310D according to a fifty seventh embodiment.

for fabricating the semiconductor device 310D can be simplified.

As shown in Fig. 127, the sealing resin forming step is carried out wherein the sealing resin 316D is formed so that the protruding terminals 330 are exposed from the sealing resin 316D. In order to easily obtain the above arrangement, the cavity surface of the mold used in the sealing resin forming step is made to come into contact with the protruding terminals 330.

The cutting positions in the cutting step are indicated by the broken lines A-A shown in Fig. 127, and are selected so that the side surfaces of the protruding terminals 330 are exposed from the sealing resin 316D. Hence, as shown in Fig. 134, the solders 354 extend up to the side surfaces of the protruding terminals 330 at the time of mounting, so that definite soldering can be realized.

A description will now be given of mounting arrangements in which the semiconductor devices 310A - 310D are mounted on the mounting board 332.

Figs. 128 through 134 show mounting arrangements of the semiconductor devices 310A - 310D according to fifty fourth through sixtieth embodiments of the present invention. A description of the following has been described and will be omitted: the mounting arrangement for mounting the semiconductor device 310A according to the fifty fourth embodiment shown in Fig. 128, the mounting arrangement for mounting the semiconductor device 310B according to the fifty sixth embodiment shown in Fig. 130, and the mounting structure for mounting the semiconductor device 310D according to the sixtieth embodiment shown in Fig. 134.

Fig. 129 shows a mounting arrangement for the semiconductor device according to the fifty fifth embodiment.

The present mounting arrangement shown Fig. 129 employs the semiconductor device 310A according to the fifty fourth embodiment by way of example, and is characterized in that mounting bumps 334 are provided to the protruding terminals 318 for external connections, and the semiconductor device 310A is bonded to the mounting board 332 through the mounting bumps 334.

By bonding the semiconductor device 310A to the mounting board 332 through the mounting bumps 334, the semiconductor device 310A can be mounted in the same manner as the BGA (Ball Grid Array) type semiconductor device, and can meet a requirement for improvement in the mounting performance and the use of an increased number of pins.

Since the protruding terminals 318 are formed on the electrode plate 314A, there is a limit on the volumes of the protruding terminals 318. However, the mounting bumps 334 are allowed to have an arbitrary volume. Hence, by maximizing the volumes of the mounting bumps 334 within a range in which the adjacent mounting bumps 334 are not short-circuited, the performance of bonding between the semiconductor device 310A and the mounting board 332 can be improved and thus the reliability thereof can be improved. The mounting arrangement of the present embodiment can be applied to the semiconductor devices 310A, 310B and 310D.

Fig. 131 shows a mounting arrangement for the semiconductor device according to the fifty seventh embodiment of the present invention.

The present mounting arrangement employs the semiconductor device 310B according to the fifty fifth embodiment by way of example, and is characterized by bonding the semiconductor device 310B to the mounting board 332 by using a mounting member 338.

The mounting member 338 is made up of

the maintenance work, the above replacement can easily be realized.

The lead parts 348 attached to the socket 344 are arranged to the sides of the attachment portion 346. Further, the side terminals 320 of the semiconductor device 310C are exposed from the sealing resin 316C. Hence, the lead parts 348 and the side terminals 320 face each other in the state in which the semiconductor device 310C is attached to the attachment portion 346. Thus, connections between the lead parts 348 and the semiconductor device 310C can be made without extending and routing the lead parts 348. Hence, the structure of the socket 344 can be simplified.

Fig. 133 shows a mounting arrangement for the semiconductor device according to the fifty ninth embodiment of the present invention.

The present mounting arrangement mounts the semiconductor device 310C on the mounting board 332 by using lead parts 350 as in the case of the mounting arrangement according to the aforementioned fifty eighth embodiment, and is characterized in that a die stage 352 is substituted for the attachment portion 346.

A socket 351 used in the present embodiment is made up of the lead parts 350 and the die stage 352, which are integrally formed by a lead frame member. The die stage 352 supports the semiconductor device 310C, and the lead parts 350 are arranged on the outer periphery thereof. The portions of the lead parts 350 that face the semiconductor device 310C are partially bent so as to be electrically connected to t he side terminals 320.

Even by using the above socket 351, the semiconductor device 310C can be attached to and detached from the mounting board as in the case of the mounting arrangement according to the fifty eighth

The heat radiating plates 356 are separated so as to have the size corresponding to that of the attachment areas 358. As shown in Fig. 138, it is possible to use joint members 360 which join the heat radiating plates 356 so that the heat radiating plates 356 are located in positions of the attachment areas 358 of the lead frame 324A.

After the above chip attachment step is completed, the chip mounting step and the protruding terminal forming step are carried out. Figs. 139 and 140 show the lead frame 324A observed after the chip mounting step and the protruding terminal forming step are completed. More particularly, Fig. 139 is a diagram of an enlarged view of a part of the lead frame 324A to which the heat radiating plate 356 is attached, and Fig. 140 shows the entire lead frame 324A.

In the chip mounting step, the heat radiating plate 356 on which the semiconductor elements 312 (312A - 321C) are attached is arranged to the lead frame 324A, so that the semiconductor elements 312A - 312C are mounted on the electrode plate 314A and are electrically connected thereto. As has been described previously, the chip attachment step of attaching the semiconductor elements 312 (312A - 312C) to the heat radiating plate 356 is executed prior to the chip mounting step. Hence, in the chip mounting step, the heat radiating plate 356 is placed on and attached to the attachment areas 358 of the lead frame 324A. Hence, the semiconductor elements 312 (312A - 312C) can be mounted on the electrode plate 314 at one time.

Hence, the chip mounting step is not required to position the individual semiconductor devices 312 (312A - 312C), but the heat radiating plate 356 having a large size and the electrode plate 314 (lead frame 324A) are merely positioned. Hence,

the positioning operation can easily be carried out.

By using the arrangement shown in Fig. 138 in which the heat radiating plates 356 are joined by the joint members 360 so as to be located in the positions of the attachment areas 358, a further increased number of semiconductor devices 312 can be positioned on the electrode plate 314 (lead frame 324A). Hence, the positioning operation can be made easier and the fabrication efficiency of the semiconductor devices 310E can be improved.

After the chip mounting step and the protruding terminal forming step are completed, the sealing resin forming step is performed. In the sealing resin forming step, the lead frame 324A to which the semiconductor elements 312 (312A - 312C) and the protruding terminals 318 are arranged is loaded onto the mold, and the sealing resin 316A is formed by the compression molding process. Since the heat radiating plate 356 is provided to the electrode plates 314A, the heat radiating plate 356 can be used as a part of the lower mold.

Fig. 141 shows the lead frame 324A to which the sealing resin 316A is formed. As shown in this figure, the sealing resin 316A is formed further in than the hear radiating member 356, so that good separating performance can be obtained. After the above sealing resin forming step is completed, the cutting step is executed so that the arrangement is cut along the lines A-A shown in Fig. 141. Thus, the semiconductor devices 310E can be obtained.

A description will now be given of a semiconductor device 310F according to a fifty ninth embodiment of the present invention.

Fig. 142 is a cross-sectional view of the semiconductor device 310F according to the fifty ninth embodiment of the present invention. The semiconductor device 310F is characterized by

formation surface of the semiconductor element 378. Hence, the protruding electrodes 380 arranged on the semiconductor element 378 are sealed by the resin layer 382 so that ends of the protruding electrodes 380 are exposed from the resin layer 382. That is, the resin layer 382 is provided to the semiconductor element 378 so as to seal the protruding electrodes 380 except for the ends thereof.

The semiconductor device main body 370 having the above structure has a chip-size package structure in which the whole size thereof is approximately equal to the size of the semiconductor chip element 378. In addition, the semiconductor device main body 370 has the resin layer 382 formed on the semiconductor element 378, the resin layer 382 sealing the protruding electrodes 380 except for the ends t hereof. Hence, the protruding electrodes 380 that are liable to be affected are protected by the resin layer 382, which has the same functions as those of the under fill resin 306.

The interposer 372A functions as an intermediate member which electrically connects the semiconductor device main body 370 and the external connection terminals 376, and is made up of a wiring pattern 384A and a base member 386A. The present invention is characterized in that a TAB (Tape Automated Bonding) tape is utilized as the interposer 372A. Generally, the TAB tape is supplied as a component of the semiconductor devices at a low cost. Thus, the cost of fabricating the semiconductor devices 310K can be reduced.

The wiring pattern 384A having the interposer 372A is, for example, a printed circuit pattern of copper. The base member 386A is formed of an insulating resin such as polyimide, and has through holes 388 located in positions corresponding to the positions the protruding electrodes 380 of the

semiconductor device main body 370.

The anisotropic conductive film 374 has a flexible resin having adhesiveness in which a electrically conductive filler is mixed. Hence, the anisotropic conductive film 374 has both the adhesiveness and electrical conductivity in the direction in which a pressure is applied. The anisotropic conductive film 374 is interposed between the semiconductor device main body 370 and the interposer 372A.

Thus, the semiconductor device main body 370 and the interposer 372A are bonded together due to the adhesiveness of the anisotropic conductive film 374. In the above bonding step, the semiconductor device main body 370 is pressed towards the interposer 372a, and is thus electrically connected to the interposer 372A by the anisotropic conductive film 374.

The external connection terminals 376 are formed by solder balls, and are connected to the wiring pattern 384A via the holes 388 formed in the base member 336A. The external connection terminals 376 is arranged on the surface opposite to the mounting surface of the semiconductor device main body 370 in order to avoid a situation in which the terminals 376 prevents mounting of the semiconductor device main body 370.

Further, the semiconductor device 310k is arranged so that the pitch at which the protruding electrodes 380 formed on the main body 370 are arranged is equal to the pitch at which the external connection terminals 376 formed on the interposer 372A are arranged. Hence, the area of the anisotropic conductive film 374 and the interposer 372A obtained when vertically viewing them is approximately equal to the area of the semiconductor device main body 370 obtained when vertically viewing it.

Since the arrangement pitch of the

protruding electrodes 380 formed on the main body 370 is equal to that of the external connection terminals 376 formed on the interposer 372A, so that the anisotropic conductive film 374 and the interposer 372A can have reduced sizes and thus the semiconductor device 310K can be down sized.

The above interposer 372A has the wiring pattern 384A formed on the base member 386A. Hence, an arbitrary pattern can be formed on the base member 386A as the wiring pattern 384A. That is, the wiring pattern 384A can arbitrarily be routed on the base member 386A.

Hence, it is possible to arbitrarily determine the positions of the external connection terminals 376 irrespective of the positions of the protruding electrodes 380 formed on the semiconductor device 370. That is, a large degree of freedom in arrangement of the external connection terminals can be obtained. Thus, it is possible to easily design the semiconductor device main body 370 and the wiring implemented on the mounting board on which the semiconductor device 310K is mounted.

As has been described previously, the anisotropic conductive film 374 has adhesiveness and electrical conductivity in the direction on which the pressure is applied. Hence, it is possible to connect the semiconductor device main body 370 and the interposer 372A by the anisotropic conductive film 374. The adhesiveness of the anisotropic conductive film 374 mechanically bonds the semiconductor device main body 370 and the interposer 372A, and the anisotropic conductivity thereof electrically bonds (connects) the semiconductor main body 370 and the interposer 372A together.

The anisotropic conductive film 374 has both the adhesiveness and conductivity, so that the number of components and the number of fabrication steps can

is urged so that it enters the connection holes 396 having a comparatively narrow size. Hence, the internal pressure in the connection holes 396 is increased.

Since the pressure exerted on the anisotropic conductive film 374 in the connection holes 396 is particularly increased, the density of the conductive filler mixed in the anisotropic conductive film 374 is also increased. Hence, the electrical conductivity of the anisotropic conductive film 374 in the connection holes 396 can be enhanced. Thus, the semiconductor device 370 and the interposer 372A can definitely be connected electrically.

Figs. 150 and 151 show a method of fabricating the semiconductor device 310L (the fabrication method according to the fifty eighth embodiment). In Figs. 150 and 151, parts that have the same structures as those shown in Fig. 148 used to describe the fabrication method according to the fifty seventh embodiment are given the same reference numbers, and a description thereof will be omitted. The following fabrication method is directed to providing a large number of semiconductor devices 310L.

First, there are prepared a wafer 390 on which semiconductor device main bodies 370 are formed, and a TAB tape 392 on which the anisotropic conductive film 374 and a plurality of interposers 372A are formed. The insulating film 394 is provided on the upper surface (on which the waver 390 is provided) of the TAB tape 392 and are located in positions facing the semiconductor device main body 370. The insulating member 394 can be formed by utilizing the photoresist formation technique. The connection holes 396 are formed in the insulating film 394 so that the holes 396 are located in positions corresponding to positions of the protruding electrodes 380.

Then, as shown in Fig. 150,, the protruding electrodes 380 and the connection holes 396 are positioned, and the anisotropic conductive film 374 is interposed between the wafer 390 and the TAB tale 392. Then, the wafer 390 is pressed towards the TAB tale 392.

Thus, the wafer 390 and the TAB tale 392 are mechanically bonded due to the adhesiveness of the anisotropic conductive film 374. Further, the protruding electrodes 380 are electrically bonded (connected) to the wiring pattern 384A due to the anisotropic conductivity of the anisotropic conductive film 374. As has been described previously, the conductivity of the anisotropic film 374 is improved within the connection holes 396. Thus, the protruding electrodes 380 and the wiring pattern 384 can definitely be connected electrically.

Fig. 151 shows a state in which the wafer 390 and the TAB tale 392 are bonded together. After the step of bonding the wafer 390 and the TAB tale 392 is completed, the cutting step is carried out in which the assembly is cut along broken lines A-A shown in Fig. 151. Hence, the individual semiconductor device main bodies 370 and the interposers 372A are formed so that a plurality of semiconductor devices 310L as shown in Fig. 149 can be obtained.

According to the present fabrication method, the mechanical bonding process and the electrically connecting process for the semiconductor device main bodies 370 and the interposers 372A can be performed simultaneously. Hence, the fabrication method for the semiconductor devices 310L can be simplified. Additionally, the present method can provide a large number of semiconductor devices 310L by a single sequence, and thus has high production efficiency.

Generally, it is said that the use of an electrical connection arrangement using an anisotropic

conductive film degrades the yield. In contrast, the present embodiments arranges the insulating member 394 in which the holes 396 are formed at the positions corresponding to the semiconductor device main body 370 (protruding electrodes 380). Hence, the electrical connections between the protruding electrodes 380 and the wiring pattern 384A can definitely be made. Thus, the semiconductor device 310L has improved reliability.

A description will now be given of a semiconductor device 310M according to a sixty sixth embodiment of the present invention.

Fig. 152 shows the semiconductor device 310M according to the sixty sixth embodiment. More particularly, Fig. 152(A) shows a cross section of the semiconductor device 310M, and Fig. 152(B) shows a bottom surface thereof. In Fig. 152, parts that have the same structures as those of the semiconductor device 310K according to the sixty fourth embodiment described with reference to Fig. 147 are given the same reference numbers, and a description thereof will be omitted.

In the semiconductor device 310K, the arrangement pitch for the protruding electrodes 380 formed on the semiconductor device main body 370 is equal to the arrangement pitch for the external connection terminals 376 arranged on the interposer 372A.

In contrast, the semiconductor device 310M is characterized in that the arrangement pitch for the external connection terminals 376 formed on an interposer 372B is greater than that for the protruding electrodes 380 formed on the semiconductor main body 370. Accordingly, the interposer 372B has an area greater than that of the semiconductor device main body 370.

Hence, it is possible to improve the degree

arrangement pitch for the protruding electrodes 380 formed on the semiconductor device main body 370 is equal to the arrangement pitch for the external connection terminals 376 provided on the interposer 372A in order to down size the semiconductor device 310N.

In contrast, in the present semiconductor device 310P, the arrangement pitch for the external connection terminals 376 provided on the interposer 372B is greater than that for the protruding electrodes 380 formed on the semiconductor device main body 370. Accordingly, the area of the interposer 372B is wider than that of the semiconductor device main body 370.

Hence, it is possible to improve the degree of freedom in routing the wiring pattern 384B on the interposer 372B. Hence, the degree of freedom in layout of the external connection terminals 376 can be improved and it becomes easy to design the layout of the terminals. Even if the protruding electrodes 380 are required to be arranged at a reduced pitch, the present arrangement can meet the above requirement.

Fig. 159 is a diagram showing a method for fabricating the above-mentioned semiconductor device 310P (fabrication method according to the sixty first embodiment). The present method is directed to fabricating the semiconductor devices 310P one by one.

First, there are prepared the semiconductor device main body 370, the adhesive 398 and the interposer 372B beforehand. The protruding electrodes 380 are coated with the conductive paste 3100 at the time of forming the semiconductor device 370. The through holes 3102 are formed in the adhesive 398 and are located in positions corresponding to those of the protruding electrodes 380. Further, the connection holes 396 are formed in the insulating member 394 and are located in the positions corresponding to those of

semiconductor device main body 370. Accordingly, the area of the interposer 372B is wider than that of the semiconductor device main body 370.

Hence, the degree of freedom in routing the wiring pattern 384B on the interposer 372B can further be improved since the external connection terminals 376 are arranged at a pitch greater than that at which the protruding electrodes 380 are arranged. Thus, the degree of freedom in layout of the external connection terminals 376 can be improved and the terminals can easily be designed. Further, the present embodiment can meet a requirement for reducing the pitch at which the protruding electrodes 380 are arranged.

Fig. 165 is a diagram showing a method for fabricating the above-mentioned semiconductor device 310Q (fabrication method according to the sixty third embodiment). The present embodiment is directed to producing the semiconductor devices 310Q one by one rather than producing them at one time.

First, the semiconductor device 370, the adhesive 398 and the interposer 372B are prepared beforehand. The through holes 3102 are formed in the adhesive 398 so as to be located in positions corresponding to those of the protruding electrodes 380. The insulating member 394 is formed to the interposer 372B, and the holes 396 are formed in the insulating member 394 so as to be located in positions corresponding to those of the protruding electrodes 380. Further, the stud bumps 3104 are formed on the wiring pattern 384A exposed in the connection holes 396 by the wire bonding technique.

Then, the positioning between the protruding electrodes 380 and the connection holes 396 is carried out, and the adhesive 398 is interposed between the semiconductor device main body 370 and the interposer 372B. Then, the semiconductor device main body 370 is pressed against the interposer 372B and is thus fixed

thereto. Hence, the semiconductor device main body 370 and the interposer 372B are mechanically bonded by the adhesive 398. The stud bumps 3104 fall in the protruding electrodes 380 through the through holes 3102 and the connection holes 396. Thus, the protruding electrodes 380 and the wiring pattern 384A are electrically bonded (connected) by the stud bumps 3104, so that the semiconductor device 310R shown in Fig. 164 can finally be obtained.

A description will now be given of a semiconductor device 310S according to a seventy first embodiment of the present invention.

Fig. 166 is a cross-sectional view of the semiconductor device 310S according to the seventy first embodiment of the present invention. In Fig. 166, parts that have the same structures as those of the semiconductor device 310N according to the sixty seventh embodiment described with reference to Fig. 154 are given the same reference numbers, and a description thereof will be omitted.

In the aforementioned semiconductor devices 310N - 310R according to the sixty seventh through seventieth embodiments, the conductive paste 3100 or the stud bumps 3104 are used, as the electrically conductive members, to electrically connect the semiconductor device main body 370 and the interposer 372A. In contrast, the present semiconductor device 310S is characterized in that flying leads 3106 (electrically conductive members) are substituted for the conductive paste 1300 or the stud bumps 3104.

The flying leads 3106 are integrally formed with a wiring pattern 384C formed in the interposer 372C, and obliquely extend upwards from the outer periphery of the interposer 372C (towards the semiconductor device main body 370). The flying leads 3106 are positioned so as to correspond to the protruding electrodes 380.

The flying leads 3106 are formed as follows. Portions of a base member 386C corresponding to the flying leads 3106 of the interposer 372C are removed by dry etching. Then, a wiring pattern 337C is obliquely bent upwards. Hence, the flying leads 3106 are formed in the outer periphery of the interposer 372C.

The flying leads 3106 bypass the positions in which the adhesive 398 is provided, and are connected to the protruding electrodes 380. Hence, the semiconductor device main body 370 and the interposer 372A are electrically connected. The positions in which the protruding electrodes 380 and the flying leads 3106 are connected are sealed by cover resins 3108. Hence, it is possible to prevent the flying leads 3106 from being deformed due to external force and to improve the reliability of the semiconductor device 310S.

As described above, in the present semiconductor device 310S, the adhesive 398 mechanically bonds the semiconductor device main body 370 and the interposer 372C, and the stud bumps 3104 electrically bond (connect) the semiconductor device main body 370 and the interposer 372C. By separately implementing the mechanical connection and the electrical connection by the respective members (adhesive 398 and the flying leads 3106), it is possible to definitely realize the mechanical and electrical connections between the semiconductor device main body 370 and the interposer 372A and to thus improve the reliability of the semiconductor device 310Q.

The adhesive 398 is not provided in the positions in which the flying leads 3106 and the protruding electrodes 380 are connected, so that the reliability of the connections therebetween can be improved. Further, the flying leads 3106 have spring

protruding electrodes 380 and the flying leads 3106 are covered. The cover resins 3108 may be formed by potting or molding. Fig. 168 shows a state in which the cover resins 3108 have been formed.

After the cover resins 3018 are formed, a cutting process is carried out so that the assembly is cut along broken lines A-A shown in Fig. 169. Hence, a plurality of semiconductor devices 310S as shown in Fig. 166 can be obtained simultaneously. Although the above-mentioned present fabrication method is directed to producing a large number of semiconductor devices 310Q at one time, it is possible to separately produce the semiconductor devices 310S one by one, as shown in Figs. 170 and 171.

A description will now be given of a semiconductor device 310T according to a seventy second embodiment of the present invention.

Fig. 172(A) is a cross-sectional view of the semiconductor device 10T according to the seventy second embodiment. In Fig. 172, parts that have the same structures as those of the semiconductor device 310N according to the sixty seventh embodiment described with reference to Fig. 154 are given the same reference numbers, and a description thereof will be omitted. In the aforementioned semiconductor devices 310N - 310S according to the sixty seventh through seventy first embodiments, the conductive paste 3100, the stud bumps 3104 or the flying leads 3106 are used as the conductive members, by which the semiconductor main body 370 and the interposers 372A or 372B are electrically bonded (connected).

In contrast, the present semiconductor device 310T is characterized in that connection pins 3110 and a positioning member 3112 are provided in an interposer 372D as conductive members rather than the conductive paste 3100 or the stud bumps 3104.

The present interposer 372D is generally

external connection terminals 376 and the protruding electrodes 380 can definitely be maintained irrespective of stress.

The connection pins 3110 are positioned so as to correspond to the protruding electrodes 380 by the positioning member 3112. Hence, the positioning process is not required which positions the connection points 3110 and the protruding electrodes 380 or the external connection terminals 376 at the time of mounting. Hence, the mounting operation can easily be executed.

Since the positioning member 3112 is formed of a flexible substance, the positioning member 3112 follows deformations of the connection pins 3110, and is thus capable of absorbing stress generated between the semiconductor device main body 370 and the interposer 372D.

Fig.s 173 through 175 show a method for fabricating the semiconductor device 310T (fabrication method according to a sixty fifth embodiment). In Figs. 173 through 175, parts that have the same structures as those shown in Figs. 155 through 157 used to describe the fabrication method of the sixtieth embodiment are given the same reference numbers, and a description thereof will be omitted. The present embodiment is directed to producing a large number of semiconductor devices 310T at one time.

First, as shown in Fig. 173, the wafer 390 on which a plurality of semiconductor device main bodies 370 are provided, the positioning member 3112 holding the connection pins 3110, the adhesive 3114 and the base member 3116. The holes 388 and the through holes 3102 are formed in the adhesive 3114 and the base member 3116 so as to be located in positions corresponding to those of the protruding electrodes 380.

for the connection pins 3110 provided in the interposer 372D.

In contrast, in the present semiconductor device 310U, the arrangement pitch for the external connection terminals 376 formed in the interposer 372B is greater than that for the protruding electrodes 380 formed on the semiconductor device main body 370. Accordingly, the area of the interposer 372B is wider than that of the semiconductor device main body 370.

Since the arrangement pitch for the external connection terminals 376 is greater than that for the protruding electrodes 380, the degree of freedom in routing the wiring pattern 384B on the interposer 372B can further be improved. Thus, the degree of freedom in layout of the external connection terminals 376 can be improved and the terminals can easily be designed. Further, the present embodiment can meet a requirement for reducing the pitch at which the protruding electrodes 380 (connection pins 3110) are arranged.

Fig. 177 is a diagram showing a method for fabricating the above-mentioned semiconductor device 310T (fabrication method according to sixty sixth embodiment). The present embodiment is directed not to producing a large number of semiconductor devices 310T at one time but separately producing semiconductor devices 310T one by one.

First, semiconductor device main body 370, the positioning member 3112 holding the connection pins 3110, the adhesive 3114 and the interposer 372B are prepared beforehand. At this time, the through holes 3102 are formed in the adhesive 3114 so as to be located in positions corresponding to those of the protruding electrodes 380.

Then, the protruding electrodes 380 and the positioning pins 3112 are positioned, and the positioning pins 3112 and the connection holes 396 are positioned. Then, the semiconductor device main body

370 is pressed against the interposer 372B while being heated. Hence, the upper ends of the connection pins 3110 fall in the protruding electrodes 380, and the lower ends thereof fall in the external connection terminals 376. Hence, the protruding electrodes 380 and the external connection terminals 376 are electrically connected together through the connection pins 3110. Thus, the semiconductor device 310U shown in Fig. 176 can be obtained.

The embodiments of the present invention have been described. The present invention is not limited to the above-mentioned embodiments, and includes various variations and modifications.